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Ph.D. Thesis

Class D audio amplifiers for high voltage capacitive transducers

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Summary (English)

Audio reproduction systems contains two key components, the amplifier and the loudspeaker. In the last 20 – 30 years the technology of audio amplifiers have performed a fundamental shift of paradigm. Class D audio amplifiers have replaced the linear amplifiers, suffering from the well-known issues of high volume, weight, and cost. High efficient class D amplifiers are now widely available offering power densities, that their linear counterparts can not match.

Unlike the technology of audio amplifiers, the loudspeaker is still based on the traditional electrodynamic transducer invented by C.W. Rice and E.W. Kellog in 1925 [1]. The poor efficiency of the electrodynamic transducer remains a key issue, and a significant limit of the efficiency of the complete audio reproduction systems. Also the geometric limits of the electrodynamic transducer imposes significant limits on the design of loudspeakers. The challenge of designing a flat loudspeaker based on the electrodynamic transducer is still not fulfilled.

Alternatives to the electrodynamic transducer based loudspeaker is the piezoelectric, horn, electrostatic and distributed-mode loudspeaker. The directivity of the electrostatic loudspeaker combined with the low level of acoustical output power and complex amplifier requirements, have limited the commercial success of the technology. Horn or compression drivers are typically favoured, when high acoustic output power is required, this is however at the expense of significant distortion combined with a large volume of the loudspeaker enclosure. Piezoelectric loudspeakers suffers from the poor power handling capability of the piezoelectric ceramic. However a niche is found in the market of hydrophones, because of the excellent impedance matching between the piezoelectric transducer and water. Distributed-mode loudspeakers represent a very interesting attempt for designing flat loudspeakers. The poor bass response combined with the diffuse and uncorrelated acoustic output, remains a challenge [2, 3].

The work presented focuses on the development of an amplifier for a special type of transducer, the DEAP (Dielectric ElectroActive Polymer) one. DEAP based loudspeakers work on the principle of the electrostatic forces, and possess some of the

same characteristics as the electrostatic loudspeaker. However, the DEAP transducer is constructed by printing compliant, corrugated electrodes on a silicone film. As a consequence a capacitive transducer emerges, which can be shaped into the loudspeaker membrane itself, rolled up into a transducer driving a membrane or being part of an active suspension system for the membrane.

In order to document the full potential of the DEAP transducer, suitable amplifiers must be developed. The frequency response and linearity of these amplifier is essential, as the application considered is that of audio. Also the efficiency of the amplifier is a key concern.

An introduction to the project is given in chapter 1, followed by a state-of-the-art study in chapter 2. Due to the similarities between the electrostatic loudspeaker and the DEAP transducer, the state-of-the-art has a special focus on amplifiers for electrostatic loudspeakers. Amplifiers for other type of capacitive transducers like piezoelectric ones are also considered. Finally the current state-of-the-art for class D audio amplifiers driving the electrodynamic transducer is presented.

Chapter 3 gives an introduction to the DEAP transducer as a load in loudspeaker systems. The main purpose being to established the frequency response of the DEAP input impedance, but also investigate the large signal implications of driving the non-linear transducer of the DEAP.

2-level modulated high voltage amplifiers driving the capacitive load of the DEAP transducer are addressed in chapter 4. An amplifier with fourth order output filter and full-state self-oscillating hysteresis based control loop is proposed. The control loop ensures high open loop gain and active damping. Active damping is a key feature in order to achieve high amplifier efficiency.

In order to further increase the output voltage or reduce the semiconductor voltage stress, multilevel inverters as amplifiers for class D audio amplifiers was introduced. The flying capacitor three-level modulated inverter is analysed, implemented and tested. A control scheme is proposed allowing for the balancing of the flying capacitor, while ensuring active damping. This subject is covered in chapter 5.

It is concluded, that class D audio amplifiers for high voltage capacitive transducers can be constructed with THD+N below 0.1 % and peak efficiency above 80 %. However the complexity of the amplifier combined with the current high cost of components, makes the technology of DEAP based loudspeaker unfeasible. Suggestions to future work in the pursuit of successful commercialisation of the DEAP technology for audio applications is given in the final chapter.

Summary (Danish)

Lydgengivelse indeholder to centrale komponenter: Forstærkeren og højtaleren. I de sidste 20 - 30 år har audioforstærkerteknologien medført et grundlæggende paradigmeskifte. Klasse D forstærkere har erstattet de lineære forstærkere, der lider af velkendte problemer som høj volumen, høj vægt og høje omkostninger. Højeffektive klasse D forstærkere er nu bredt tilgængelige, og tilbyder effekttætheder ingen af deres lineære modstykker kan matche.

I modsæting til audioforstærkeren er højtaleren stadig baseret på den traditionelle elektrodynamiske transducer, opfundet af C.W. Ris og E.W. Kellog i 1925 [1]. Den elektrodynamiske transducers lave effektivitet er et centralt problem, og en betydelig begrænsning i effektiviteten af det samlede lydgengivelsessystem. Også de geometriske begrænsninger for den elektrodynamiske transducer pålægger designet af højtaleren betydelige restriktioner. Udfordringen i at designe en flad højtaler, baseret på den elektrodynamiske transducer, er således stadig ikke opfyldt.

De eksisterende alternativer til den elektrodynamiske højtaler er piezoelektriske højtalere, horn højtalere, elektrostatiske højtalere og distribueret mode højtalere. Direktiviteten af den elektrostatiske højtaler kombineret med den lave akustiske udgangseffekt og de komplekse forstærker krav, har begrænset den kommercielle succes af teknologien. Horn højtalere anvendes typisk når høj akustisk udgangseffekt er påkrævet. Dette sker dog på bekostning af en betydelig forvrængning. Piezoelektriske højtalere lider under den lave elektriske effekt, som den piezoelektriske keramik kan håndtere. En niche findes på markedet for hydrofoner, grundet den fordelagtige impedans matching mellem den piezoelektriske transducer og vand. Distribueret mode højtalere repræsenterer et meget interessant forsøg på at designe flade højtalere, men det dårlige bas response kombineret med et diffus og ukorreleret akustisk output, er fortsat en udfordring [2, 3].

Arbejdet præsenteret i denne afhandling fokuserer på udvikling af en forstærker til en særlig type transducer, nemlig DEAP (Dielektrisk ElektroAktiv Polymer) transdueren. DEAP baseret højtalere arbejder på princippet om de elektrostatiske kræfter, og har nogle af de samme egenskaber som den elektrostatiske højtaler. Transduceren kon-

strueres ved at printe eftergivende, bølgende elektroder på en silikone film. Som følge heraf opnås en kapacitiv transducer, der kan udnyttes som selve højtalermembranen, eller rulles op til en transducer der driver højtalerens membran.

For at dokumentere det fulde potentiale af DEAP transduceren, skal egnede forstærkere udvikles. Frekvensgangen og lineæriteten af disse forstærkere er af afgørende betydning, da applikationen er audio. Også effektiviteten af forstærkeren er et centralt emne.

En introduktion til projektet er givet i kapitel 1, efterfulgt af en state-of-the-art undersøgelse i kapitel 2. På grund af lighederne mellem den elektrostatiske højtaler og DEAP transduceren, fokuserer state-of-the-art kapitlet på forstærkere til den elektrostatiske højtaler. Forstærkere til andre typer af kapacitive transducere, såsom piezoelektriske, betragtes også. Endelig vil den nuværende state-of-the-art, for klasse D audio forstærkere der driver elektrodynamiske transducere, blive præsenteret.

Kapitel 3 giver en introduktion til DEAP transduceren som en belastning i højtalersystemer. Hovedformålet er at etablere frekvensresponset for DEAP'ens indgangsimpedans, men også at undersøge konsekvenserne af DEAP transducerens ulineæriteter.

2-niveau moduleret højspændingsforstærkere som drivere for den kapacitive belastning af DEAP transduceren er behandlet i kapitel 4. En forstærker med 4. ordens udgangsfilter og fuld tilstandsvariable selvoscillerende hysteresis baseret kontrol-loop er præsenteret. Kontrol-loopet sikrer en høj åben-sløjfeforstærkning og aktivdæmpning. Aktivdæmpning er et centralt element for at opnå en høj effektivitet for forstærkeren.

For yderligere at øge spændingen eller reducere halvleder-spændingsstresset, blev multilevel inverters som klasse D audio forstærkere indført. Den flyvende kondensator 3-niveau moduleret inverter er analyseret, implementeret og testet. Et kontrol-loop som tillader balancering af den flyvende kondensator, samt aktivdæmpning, er præsenteret. Disse emner behandles i kapitel 5.

Det konkluderes, at klasse D audio forstærkere til højspændings kapacitive transducere kan konstrueres med THD+N under 0.1 % og med maksimal effektivitet over 80 %. Kompleksiteten af forstærkeren kombineret med de nuværende høje omkostninger til komponenter, gør dog DEAP højtalerteknologien urentabel. Sidste kapitel indeholder en række forslag til fremtidigt arbejde i den videre forfølgelse af DEAP teknologien indenfor området audio.

Preface

This thesis is submitted in partial fulfillments of the requirements for obtaining the PhD degree under the PhD research program EnergyLabDK at the PhD school of the Technical University of Denmark, DTU Elektro, Electronics Group. The work was supported by The Danish National Advanced Technology Foundation (ATF) under the project number 009-2011-2. A joint research cooperation between the primary partners of Danfoss PolyPower A/S, DTU Elektro and Bang & Olufsen A/S was conducted. During the project, a research visit was carried out at "Department of Electrical, Computer, and Systems Engineering" at Rensselaer Polytechnic Institute, USA.

Acknowledgment

A special thanks goes to

- My dear girlfriend and family for their love and never ending support during this project.
- My supervisors, Michael A. E. Andersen and Arnold Knott for giving me this opportunity and their support.
- Erik Bruun for his support during the final part of the project.
- All of my colleagues and students for their support and constructive discussions.

Contents

CHAPTER 1

Introduction and motivation

1.1 Scope

The scope of this thesis is to present the research obtained in the PhD project "Class D amplifiers for capacitive transducers", carried out during the period from August 2011 through October 2014. The scientific results of the research have been published in form of peer reviewed conference papers. A publication list of the PhD study can been found in appendix A.

The objective of this thesis is to supplement the already published information. Given a coherent and complete overview of the work and results obtained in during project.

The thesis includes a large number of advanced knowledge of amplifier design and control theory in power electronics. It is a hope that the thesis is useful to those power engineers, who are working within the field of audio amplifiers.

1.2 Background and Motivation

The project originates from the Dielectric Electro Active Polymer (DEAP) transducers developed by Danfoss Polypower A/S. Danfoss Polypower A/S has spend several years developing the DEAP technology [4] and are now ready to target commercial applications. The main advantages of the DEAP technology are very low electrical power consumption, no noise, higher performance than competing technologies and low weight [5].

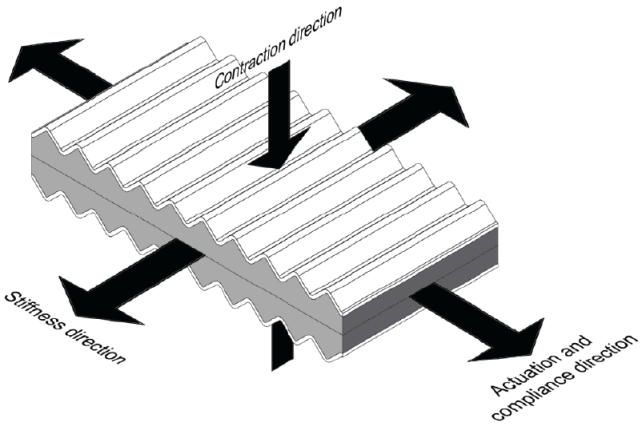


Figure 1.1: Anistropic properties [10].

A DEAP film is constructed by printing compliant electrodes on opposite surfaces of a thin dielectric material (typically silicone). The electrostatic force between the electrodes is utilised to compress the dielectric material in the thickness direction, causing an in-plane expansion. A DEAP can sometimes be found in the literature under the name "artificial muscles" [6].

One of the key challenges of the DEAP technology is to control the in-plane expansion. In order to handle this challenge the concept of 3D anisotropic corrugated compliant metallic electrodes has been introduced [5]. Figure 1.1 illustrates the concept. An anisotropic material possess properties depended upon the direction. The electrodes have a sinusoidal-like form causing the direction transverse to the corrugation direction being stiff, while the direction of the corrugation is compliant. Assume a constant volume of the polymer material, the electrically induced stress in the direction of the film thickness, will be converter into mechanical stews in the direction of corrugation [7]. The corrugation length, deepth and film thickness are typically measured in micrometers, while the thickness of the metal electrodes is measured in nanometers. This ensures a suitable trade off between not adding unwanted stiffness to the polymer, maintaing conductivity and allowing for large displacements [8].

The tubular DEAP actuator can be constructed by rolling the DEAP film with the compliant direction along the axial axis as shown in figure 1.2. This type of actuator is the most common DEAP based actuator found in the literature [9].

This Ph.D. project is part of a larger ATF project under The Danish National Advanced

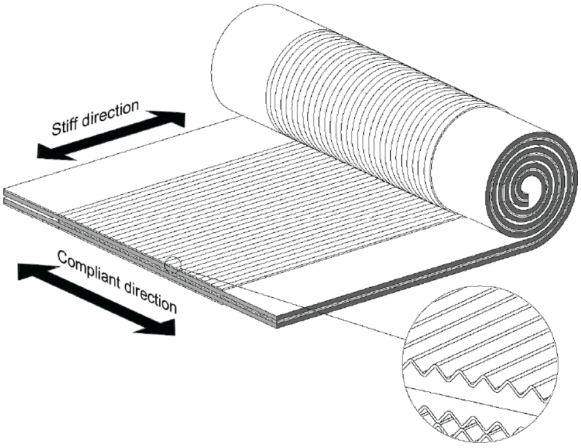


Figure 1.2: Corrugated film [10].

Technology Foundation [11]. The project is headed by Danfoss PolyPower A/S. An overview of the entire ATF project is given in figure 1.3. The ATF project spans across research in polymer material, optimisation of production facilities, design of DEAP components and four lead applications (incremental motor, wave energy harvesting, electric value and loudspeakers). This Ph.D. project is attached to work page (WP) 4 - High voltage power electronics in close collaboration with WP 9 - Flat screen loudspeaker. The goal of the Ph.D. project is to design high voltage amplifiers suitable for driving the DEAP based loudspeakers developed by Bang & Olufsen A/S. Bang & Olufsen A/S considers the DEAP film as an opportunity to develop new transducer and membrane structures having a different form-factor than those found in the traditional electrodynamic based loudspeaker. Improving the overall systems efficiency of the loudspeaker and amplifier setup is of key interest as well. This being a common task of WP 4 and WP 9.

1.3 Project Objectives

- Characterisation of DEAP loudspeakers from a load perspective. This research will give a clear insight into the properties of the DEAP loudspeaker from an electrical point of view using large- and small-signal modelling.
- Like conventional audio amplifiers suitable power stages must be identified and analysed. The goal is to reach audio quality in terms of THD+N (below 0.1 %), together with high efficiency and power density.

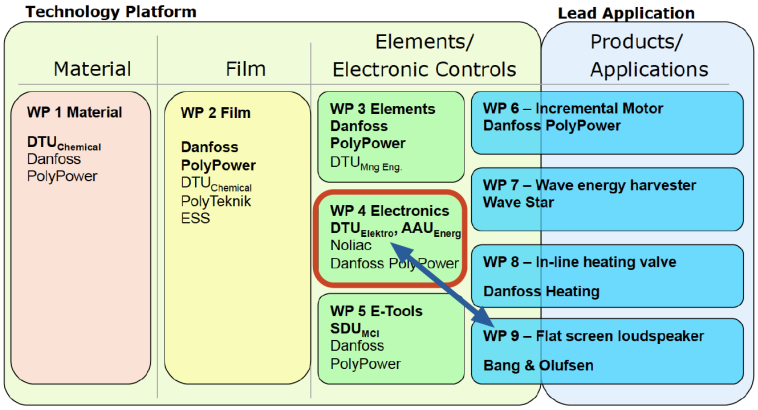


Figure 1.3: Overall ATF project [11].

- Suitable control methods is to be identified and implemented. The high impedance of a DEAP transducer imposes new challenges, which must be solved.

The DEAP transducer needs to operate under the influence of a biasing voltage. Implementation of such a biasing source, and the DC supply needed to drive the audio amplifier, is not considered in the thesis. It is assumed, that the results of the research on the amplifier part can be directly correlated with the appropriate DC supplies.

1.4 Thesis Structure and Content

The flow chart of figure 1.6 gives a visual presentation of the PhD thesis structure. Conference papers are included in the flow chart with relation to specific scientific subjects. The purpose of this report is to complement the papers by providing a condensed and coherent presentation of the overall project. Special focus will be devoted to the presentation of key fundamental theoretical aspects of this project together with the validated results.

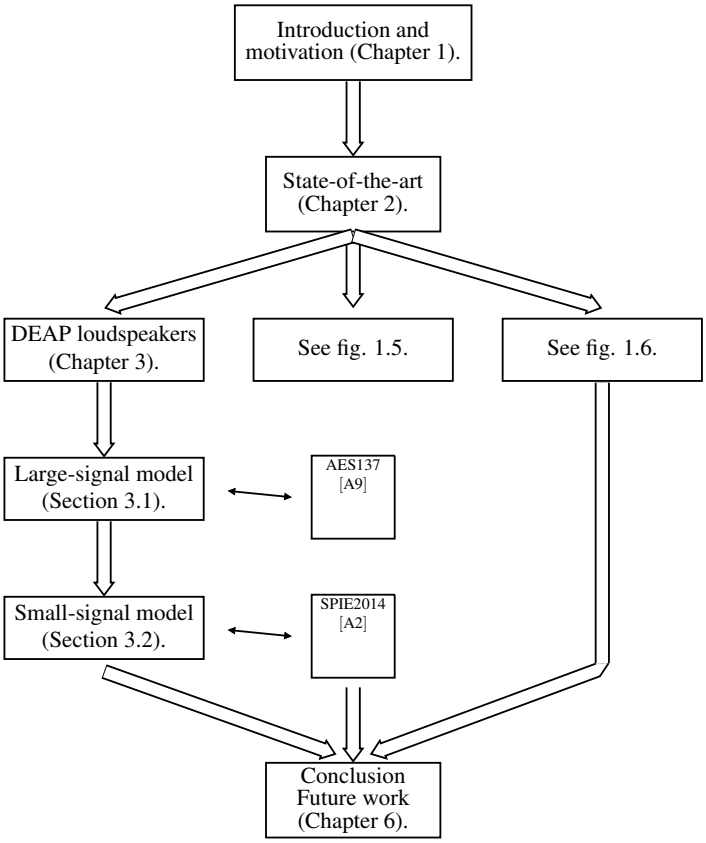


Figure 1.4: Flow chart of thesis structure.

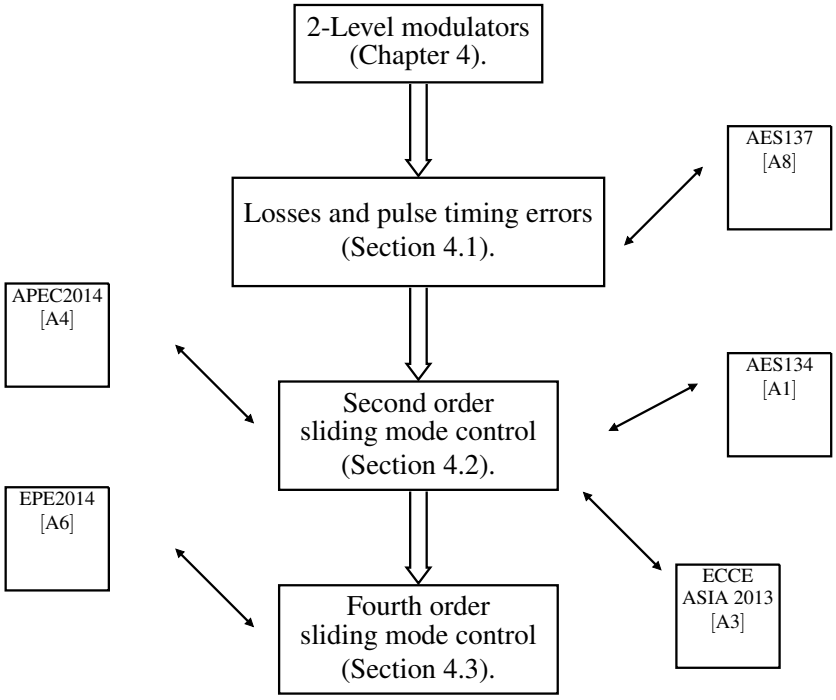


Figure 1.5: Flow chart of thesis structure (continued).

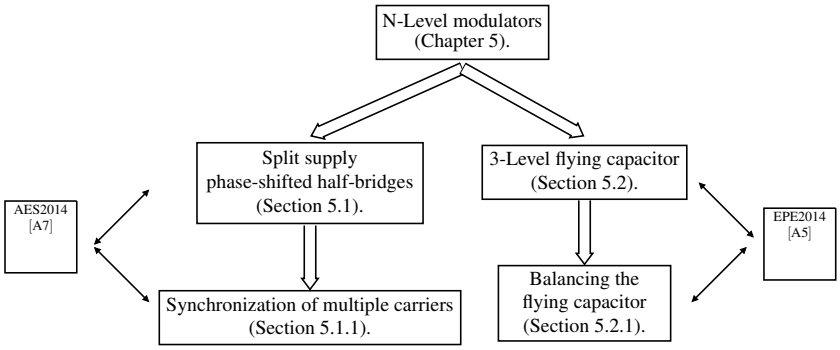


Figure 1.6: Flow chart of thesis structure (continued).

CHAPTER 2

State-of-the-art

DEAP, piezoelectric and electrostatic transducers all represent high voltage, capacitive loads to their amplifiers [12, 13]. The purpose of this chapter is to provide an overview of the state-of-the-art within the area of amplifiers for these capacitive transducers. Because this area historically has seen very little commercial success, amplifiers suitable for driving restive and inductive loads are also considered. The focus is placed upon amplifiers and control schemes. While the application of audio is the main interest, applications like motor drive and robotics are also considered in order to illustrate the full solution space [14]. Figure 2.1 illustrates the solution tree, which will be investigated in the following sections. However before proceeding with this subject, an overview of the current state-of-the-art within class D audio amplifiers driving the resistive and inductive load of the electrodynamic loudspeaker is presented. The purpose being to establish a benchmark of which audio amplifiers for capacitive transducers could be measured.

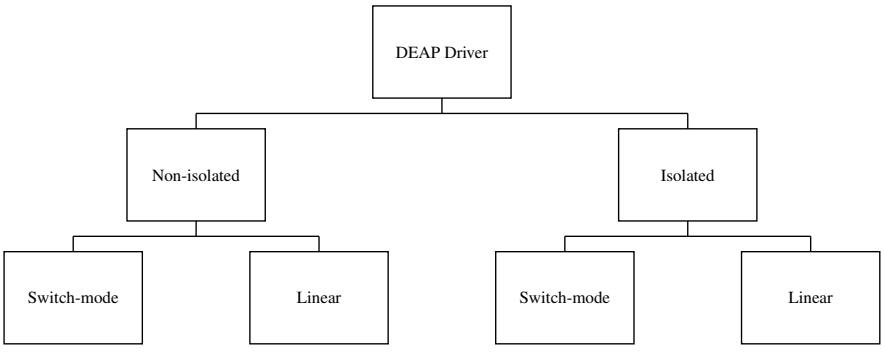


Figure 2.1: Solution tree.

2.1 Class D audio amplfiers

Class D audio amplifiers have gained huge commercial success in the last 20 – 30 years. Commercial available class D amplifiers are based upon the full- and half-brigde power stages as shown in figure 2.2 and figure 2.3. These amplifiers can typically deliver 90 – 1200 W of peak power into a resistive load of 2 – 8 Ω. THD+N below 0.1 % across the operating range is commonly achieved [15, 16, 17].

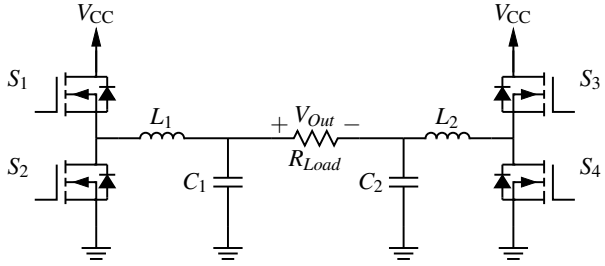


Figure 2.2: Full-bridge (FB) class D power stage.

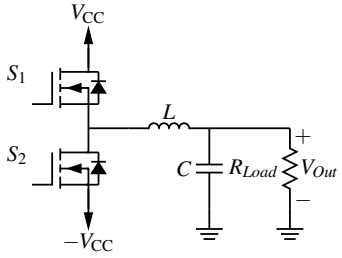


Figure 2.3: Half-bridge (HB) class D power stage.

Table 2.1 and 2.2 gather a selection of class D audio amplifiers found in the literature. Commercial available class D amplifiers includes [16], [24] and [15]. Note that the stated efficiency of [15] is that of the complete amplifier with power supply operating from the mains, while the efficiency of [16] and [24] is of the amplifier itself. The full- and half-brigde power stages have historically prevailed [25, 26], due to their high linearity (proportional relation between the output and input voltage) and lack of right half-plane zeroes. Research into non-proportional gain power stages for class D audio amplifiers have been conducted in [27, 28, 23, 29, 30]. Buck-Boost, Double-Boost and Cuk power stages are used to target the application of switch-mode based amplifiers for portable devices. Little to none measuring results are reported, and no commercial success is found.

The system level block diagram of a mains operated class D amplifier is shown in

Reference	THD+N [%]	Maximum efficiency [%]	Peak Power [W]
[18]	0.023[a]	–	100
[19]	0.02[b]	–	300
[20]	0.05[a]	–	125
[21]	0.05[b]	–	95
[22, 16, 17]	0.0015[c]	93	1200
[23]	0.5[d]	75	100
[24]	0.03[a]	90	300
[15]	0.12[a]	79	1175

[a] 4 Ω, M = 0.75 and 6.67 kHz
[b] 8 Ω, M = 0.75 and 6 kHz
[c] 2 Ω, M = 0.75 and 6 kHz
[d] 8 Ω, M = 0.75 and 6.67 kHz

Table 2.1: State-of-the-art within class D amplifiers driving electrodynamic loudspeakers.

Reference	Control strategy	Power stage	Switching frequency [kHz]
[18]	Hysteretic SO[a], BPCM+PI[b]	HB[c], ± 34 V	350
[19]	Fixed-freq. PWM with MAE[d] filter	FB[e], 55V	350
[20]	Hysteretic SO, GLIM[f]	HB, ± 40 V	350
[21]	One-cycle	FB, 54 V	250
[22, 16, 17]	NCore, SO with complex poles	HB, ± 105 V	500
[23]	Hysteretic SO, GLIM	SICAM	150
[24]	SO, HCOM[g]	FB, 55 V	480
[15]	MECC[h], COM[i]	FB, 120 V	350

[a] Self-Oscilation.
[b] Bandpass Current Mode plus Proportional Integral
[c] Half-Brigde
[d] Minimum Aliasing Error
[e] Full-Brigde
[f] Globale Loop Integratal Modulator
[g] Hybrid feedback Controlled Oscillation Modulator
[h] Multivariable Enhanced Cascade Controlled
[i] Controlled self-Oscilating Modulator

Table 2.2: State-of-the-art within class D amplifiers driving electrodynamic loudspeakers (continued).

figure 2.4 [23]. A separate DC supply ensures the proper operating voltage of the class D amplifier. The SIngle Conversion stage AMplifiers (SICAM) for audio applications is analysed in [23] and proposed as an alternative to the DC-link approach. Using High Frequency (HF) -linked transformers class D amplifiers was build as single stage conversion operating directly from the mains. The complexity of both the power stage and control scheme showed, that SICAM amplifiers had significant problems with the noise floor, and could not compete with the full- and half-bridge in terms of THD+N. Also the HF-link power stage needs bidirectional switches on the secondary side. Figure 2.5 shows the SICAM power stage using a full-bridge power stage. A flyback version of the SICAM is also found in [23].

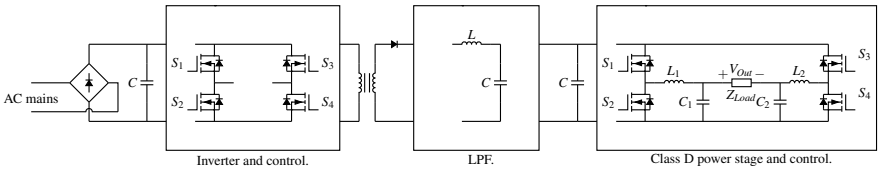


Figure 2.4: Traditional class D amplifiers operating from mains.

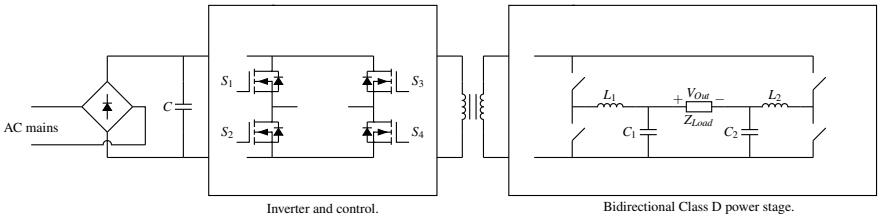


Figure 2.5: SICAM.

2.2 Linear amplifiers

2.2.1 Galvanically non-isolated

Linear amplifiers include the class A, B, AB, C, G etc. [23, 25]. This category of amplifiers has been proposed as drivers for both piezoelectric transducers and electrostatic loudspeakers. Some authors have taken on the task of analysing and comparing capacitive loaded amplifiers [31, 32, 33]. However before proceeding it is appropriate to give a formal definition of the term efficiency. The energy efficiency when charging

a capacitive load will be defined as [10]

$$\eta_{Charge} = \frac{E_{DEAP}}{E_{In}} \tag{2.1}$$

$$= \frac{\frac{1}{2}C_{DEAP}V_{DEAP}^2}{\int \mathrm{V_{In}(t)I_{In}(t)d}t} \tag{2.2}$$

With E_{DEAP} being the energy delivered to the capacitive DEAP transducer, and E_{In} the input energy of the amplifier.

During discharge the energy efficiency is

$$\eta_{Discharge} = \frac{E_{In}}{E_{DEAP}} \tag{2.3}$$

$$= \frac{\int \mathrm{V_{In}(t)I_{In}(t)d}t}{\frac{1}{2}C_{DEAP}V_{DEAP}^2} \tag{2.4}$$

as the energy is returned to the supply of the amplifier, assuming the amplifier is capable of handling bidirectional flow of energy.

When driving a capacitive transducer with sinusoidal waveforms, the efficiceny can be convenient defined in terms of the reactive power circulated by the converter with respect to the real power loss [14]

$$\eta = \frac{P_{Out}}{P_{Out} + P_{Loss}} \tag{2.5}$$

where $P_{Out} = \omega C_{DEAP}V_{rms}^2$, the reactive power delivered to the load, and P_{Loss} corresponds to the real power consumed by the amplifier.

Let us consider the ideal Class B amplifier as representative of the linear amplifiers. A Class AB amplifier would probably be preferable in all practical applications, however the inclusion of quiescent losses is beyond the scope of this simple 1. order analysis. Assuming $v_{Out}(t) = V_{Bias} + \hat{V}cos(\omega t)$ and $i_{Out}(t) = \hat{V}C_{DEAP}\omega sin(\omega t)$, the input power of the Class B amplifier shown in figure 2.6 can be calculated as the sum of power loss in Q_1 and Q_2

$$P_{Loss} = P_{Q1} + P_{Q2} \tag{2.6}$$

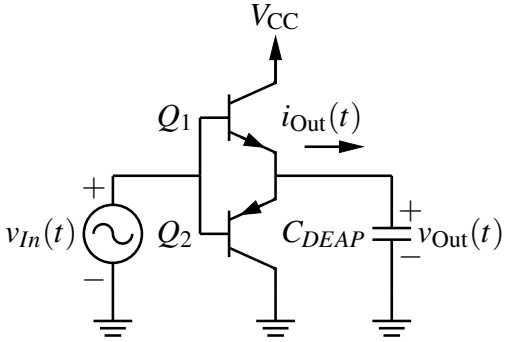


Figure 2.6: Class B amplifier with capacitive load.

with

$$P_{Q1} = \frac{\omega}{2\pi}\int_0^{\frac{\pi}{\omega}}(V_{CC}-v_{Out}(t))i_{Out}(t)\mathrm{d}t \tag{2.7}$$

$$= \frac{\omega}{2\pi}\int_0^{\frac{\pi}{\omega}}(V_{CC}-V_{Bias}-\hat{V}cos(\omega t))\hat{V}C_{DEAP}\omega sin(\omega t)\mathrm{d}t \tag{2.8}$$

$$= \frac{\omega\hat{V}C_{DEAP}V_{Bias}}{\pi} \tag{2.9}$$

and

$$P_{Q2} = \frac{\omega}{2\pi}\int_{\frac{\pi}{\omega}}^{\frac{2\pi}{\omega}} v_{Out}(t)i_{Out}(t)\mathrm{d}t \tag{2.10}$$

$$= \frac{\omega}{2\pi}\int_{\frac{\pi}{\omega}}^{\frac{2\pi}{\omega}}(V_{Bias}+\hat{V}cos(\omega t))\hat{V}C_{DEAP}\omega sin(\omega t)\mathrm{d}t \tag{2.11}$$

$$= \frac{\omega C_{DEAP}\hat{V}(V_{CC}-V_{Bias})}{\pi} \tag{2.12}$$

The efficiency then becomes

$$\eta = \frac{\frac{\hat{V}^2\omega C_{DEAP}}{2}}{\frac{\hat{V}^2\omega C_{DEAP}}{2}+\frac{\omega C\hat{V}V_{CC}}{\pi}} \tag{2.13}$$

$$= \frac{\frac{\hat{V}}{2}}{\frac{\hat{V}}{2}+\frac{V_{CC}}{\pi}} \tag{2.14}$$

For $\frac{V_{CC}}{2} = \hat{V}$ the efficiency reaches its maximum

$$\eta_{Max} = \frac{\pi}{\pi+4} \tag{2.15}$$

The theoretical maximum efficiency of $\frac{\pi}{\pi+4} = 44.0\%$ for the class B amplifier, justifies the pursuit of a switch-mode amplifier as the DEAP driver. Notice that a class B amplifier driving a capacitive load will have a significant smaller efficiency than the 78% maximum efficiency of one driving a resistive load [25]. A 220 V class B amplifier, diving a 12 uF load at 10 Hz, having an energy recovery of 26.8 %, together with an improved class B amplifier producing an energy recovery of 35.2 %, is presented in [32]. The improved class B is implemented using a capacitive buffer between the load and BJT power stage, limiting the loss associated with circulating the energy back through the BTJs to the supply.

Another observation is to be made. The energy efficiency of the linear amplifier is independent of frequency. This is interesting as the reactive output power for a purely capacitive load will change with frequency, assuming voltage mode control.

A linear tube based amplifier is found in [34]. Tubes allow the amplifier to operate at 5 kV, however tube based amplifiers suffer from being very fragile, heat sensitive and the inherent low efficiency of the linear power stage.

2.2.2 Galvanically isolated

Capacitive transducers used currently in audio applications include the condenser microphone and electrostatic loudspeaker. Both working on the principle of the electrostatic forces [35]. The properties of the electrostatic loudspeaker and the DEAP based loudspeaker can thus be considered somewhat identical. However it should be stressed, that the electrodes of the DEAP loudspeaker are corrugated with a dielectric polymer material (silicone) between them, while the electrostatic loudspeaker have flat electrodes separated only by the air.

Electrostatic loudspeakers are commercial available from Quad and Martin Logan. Figure 2.7 are pictures of two electrostatic loudspeakers. From an amplifier point of view, special attention should be given to the bottom box of these loudspeakers. In order to interface with traditional audio amplifiers design for the inductive and resistive load of the electrodynamic transducer, electrostatic loudspeakers have build-in step-up circuitry, which ensures the high operation voltage (audio and biasing component). Schematic of the step-up circuitry of the Quad loudspeakers are found in [3]. The concept is illustrated in figure 2.8 showing, that an audio transformer is utilised to step-up

(a) Quad [36]. (b) Martin Logan [37].

Figure 2.7: Commercial electrostatic loudspeakers.

the audio component, while a separate source ensures biasing. The later implemented using voltage multipliers.

2.3 Switch-mode based amplifiers of capacitive transducers

2.3.1 Proportional gain

Proportional gain switch-mode based amplifiers for capacitive transducer is primarily found in the literature in the form of the full- and half-bridge as amplifiers for piezoelectric transducers [38, 39, 40]. A driver for the parametric loudspeaker is patented in [41]. The parametric loudspeaker being an ultrasound loudspeaker, which can be implemented using an electrostatic or piezoelectric transducer. Multilevel operation is also covered by the patent. Self-oscillating control loop using both current and voltage feedback is patented in [42]. Class D amplifiers have been proposed as drivers of electrostatic loudspeakers in [43]. Open loop operation is considered, and a step-up audio transformer is added to the output filter of the amplifier, if an operating voltage higher than allowed by the MOSFETs is needed. A high voltage switch-mode based

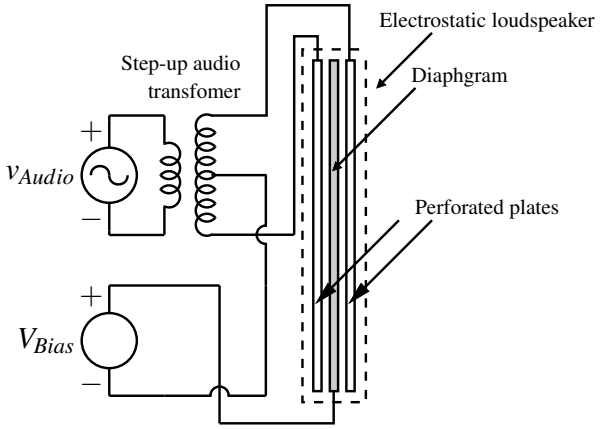


Figure 2.8: Electrostatic loudspeaker in push-pull mode with build-in step-up audio transformer and separate biasing circuit [3].

direct drive for electrostatic loudspeakers is presented in [44][1], however no THD+N or efficiency measurements are shown.

A switched capacitor power stage is proposed in [45] as amplifier for a piezoelectric transducer, however experimental results do not address the linearity nor the efficiency.

2.3.2 Non-proportional gain

Non-proportional gain power stages have been proposed as amplifiers for DEAP and piezoelectric transducers in robotic and valve applications [46, 47, 48, 49, 50, 51, 52, 53, 54, 14, 12]. These include the boost and flyback amplifier. Bidirectional operation is essential in order to ensure high discharge efficiency with figure 2.9 showing the bidirectional version of a flyback amplifier. Charging efficiency above 90 % and discharge efficiency of 70 % have been reported operation with a peak output voltage of 2.25 kV [55]. Limitations in current handling abilities, causes these amplifiers to be unsuitable for the application of audio. The presence of right half-plane zeroes and the non-proportional gain, further complicates the control-loop design of such amplifiers.

Danfoss Polypower offers a switch-mode based amplifier for their DEAP sample kit [56]. The amplifier is transformer based, and can charge a capacitve load up to 2.5 kV. Maximum operating frequency is 10 Hz, limited by the current.

[1] $\pm 375V$ supply full-bridge

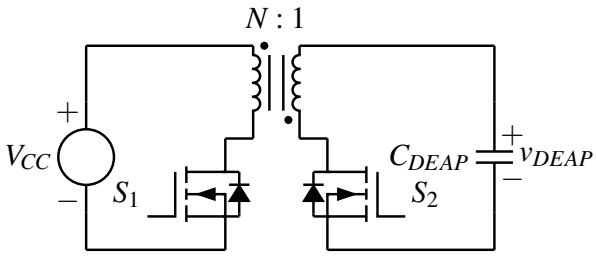


Figure 2.9: Bidirectional flyback.

Non-isolated dual stage configurations can be found in [14, 57]. Boost converters are used to ensure the required voltage for the half-bridge output power stage. These configurations is most suitable for operating from a battery as these are non-isolated. The amplifier of [57] is shown in figure 2.10.

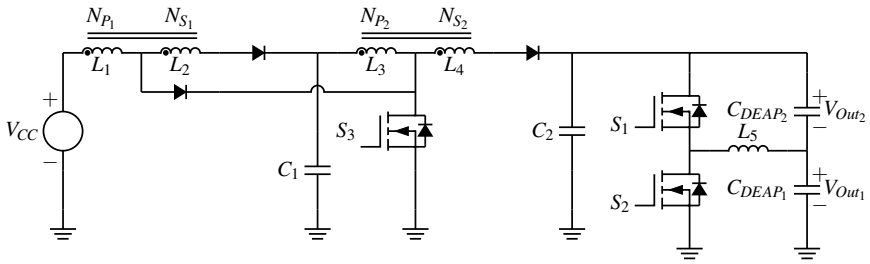


Figure 2.10: Non-isolated dual stage amplifier with capacitive transducers operating in push-pull mode as proposed in [57].

Amplifiers for DEAP transducers based on piezoelectric transformers (PT) are investigated in [58, 59, 60]. These amplifiers achieved high power density, however the piezoelectric transformer are not suitable for handling the current needed to drive a DEAP transducer within the audio band. Bidirectional implementation is complicated by the highly capacitive secondary side. The resonance converter nature of piezoelectric transformers based amplifiers calls for pulse density or burst mode modulation, which combined with the resonance frequency of typically 100 kHz, significantly limits the frequency response [25]. Figure 2.11 shows the bidirectional half-bridge based amplifier using a piezoelectric transformer as analysed for the DEAP application in [10, 61]. It is illustrated in figure 2.12, that the piezoelectric transformer based amplifier can be made small enough to fit inside the hollow space of the tubular DEAP transducer. A charge efficiency of 59 % is reported in [10], when charging a 47 nF load from 0 to 2 kV. The height of the amplifier in figure 2.12 is 7.1 mm, while the width is 95mm and the depth is 13 mm. Charging and discharging cycles are conducted at a frequency of 2 Hz, and thus fare below the bandwidth requirements of an

audio amplifier.

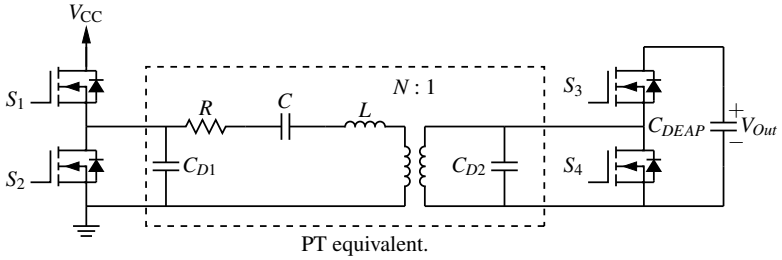


Figure 2.11: Piezoelectric transformer with half bridge power stage.

2.3.3 Control

Control schemes for switch-mode converters can be divided into the categories [62, 63]:

- Voltage-mode, current-mode (average/peak) or charge-mode.
- Fixed or variable frequcency.
- Linear or non-linear.
- Synchronised or self-oscillating.
- Analog or digital.
- Single phase or phase shifted.

The analog control in the form of fixed frequency or self-oscillation[2] is typically found in high performance power amplifiers [15, 16, 17, 24]. Digital control in class D audio amplifiers is used in applications like haring aids implemented through sigma delta converters [64]. Complex interpolation filters and noise shapers is necessary in order to deal with the practical limits in the clock frequency. A true comparison between the analog and digital control including performance- and cost-functions is yet to be seen. The high loop delay in global modulated digital class D amplifiers is also a concern due to stability issues [65, 25].

Charge and current mode control schemes have been proposed for amplifiers of capacitive loads such as the electrostatic loudspeaker and piezoelectric transducer [66]. The

[2] Also known as sliding mode control.

Figure 2.12: Piezoelectric based DEAP driver [10].

benefit of these control schemes is, that the linearity of the electrostatic transducer is improved [3], however at the expense of the displacement. Voltage mode operation is thus typically selected for applications in the need of maximum displacement.

One cycle control is together with self-oscillation examples of non-linear control schemes [25]. The one cycle control scheme has demonstrated excellent performance in terms of THD+N [21]. Table 2.1 and 2.2 does however illustrate, that self-oscillation control schemes are the predominant choice for class D audio amplifiers driving the electrodynamic transducer [18].

Self-oscillating control schemes are implemented as either phase or hysteresis based modulators [26, 22, 16, 17]. A disadvantage of the self-oscillating control scheme is the change in switching frequency with modulation index. A hysteresis based modulator using spike synchronisation is proposed in [67], however the cross-over frequency of the comparator frequency response is half that of the comparable standard hysteresis comparator modulator [62].

Single phase control is found in class D audio amplifiers using the half-bridge power stage [25, 26]. Class D audio amplifiers using a number of half-bridges connected in parallel in order to achieve higher orders of modulation uses phase shifted control [25]. The three-level modulated full-bridge is an example of this. Also bidirectional resonance converters uses phase shifted control in order to ensure the proper direction of the power flow [10].

2.4 Summary

This chapter has established the present state-of-the-art of drivers for capacitive transducers through a literature review. Currently, little to none switch-mode based drivers

for capacitive transducers are available capable of handling high voltage operation and the frequencies within the audio band. The current state-of-the-art within class D audio amplifiers driven the electrodynamic transducer is established. Analyses of the linear amplifier under a capacitive load is conducted. It is shown, that the energy efficiency of the linear amplifier is independent of the frequency.

CHAPTER 3

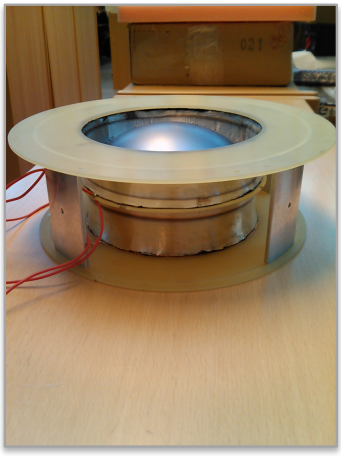
DEAP loudspeakers

The purpose of this section is to describe the DEAP loudspeaker as a load from an amplifier perspective. A complete acoustical and mechanical analysis of the DEAP loudspeaker is beyond the scope of this thesis, and related to WP 9 of the ATF project (see figure 1.3). Impedance measurements is used to document the load, that the amplifier is to drive. Large-signal analysis is preformed using the electrostatic pressure in a planar sheet of DEAP [68].

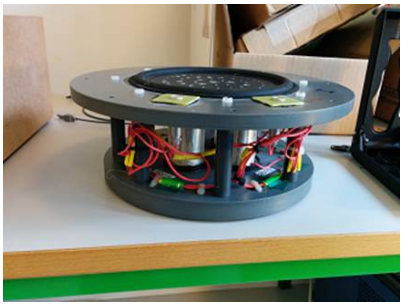
3.1 Large-signal model

DEAP in loudspeaker applications was demonstrated for the first time in 1998 [69]. A single layer polymer film suspended in a quadratic form confirmed that there are challenging problems regarding distortion. In 2000, an SPL of 80 dB was achieved, again using single layer DEAP film [70].

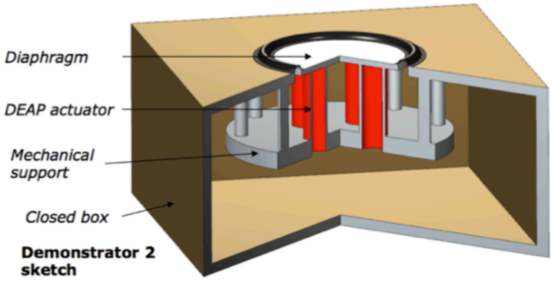
During the project two demonstrator loudspeakers have been developed by Danfoss PolyPower and B&O. These are shown in figure 3.1. The loudspeaker of figure 3.1(a) work on the principle of push-pull. Inspired by the work of [71, 72], the DEAP film is wound into a cylinder with a membrane attached in the cross-sectional area. Electrically the DEAP film is divided into a DEAP transducer above the membrane, and a DEAP transducer below the membrane. Operating the two DEAP transducers at a phase of 180 ^{o}, they will push and pull the membrane, respectivly. The configuration inherently enables mechanical pre-strain of the DEAP transducers (5 % – 10 %). Figure 3.1(c) and 3.1(b) shows a push configuration, having 4 DEAP transducers connected in parallel with a membrane attached on top.



(a) Push-pull loudspeaker [73].



(b) Push loudspeaker without box [74].



(c) 3D model of Push loudspeaker [74].

Figure 3.1: DEAP loudspeakers.

3.1.1 Electric model

The electrical model of the DEAP transducer is a variable capacitor having a series and parallel resistance as illustrated in figure 3.2 [75, 76].

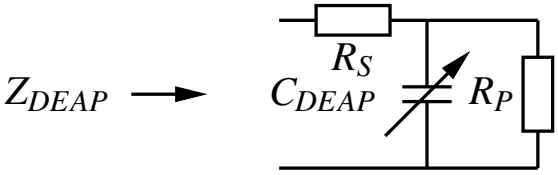


Figure 3.2: Electrical model.

The variable capacitor of figure 3.2 is denoted the static DEAP capacitance, and is a function of the biasing voltage. Before looking at the dependency of the biasing voltage, first consider the measured impedance of the push loudspeaker at zero biasing as shown in figure 3.3. The impedance of the push loudspeaker has an electrical resonance at 150 kHz. As a consequence the DEAP transducer is not a suitable choice for the output filter capacitor in a class D amplifier with switching frequencies in the region of 100 kHz or above. The electrical model of the DEAP transducer can be extended to include the inductive part of the impedance. However, for frequencies in the midrange of the audio band (100 – 3.5 kHz), the model of figure 3.2 is sufficient.

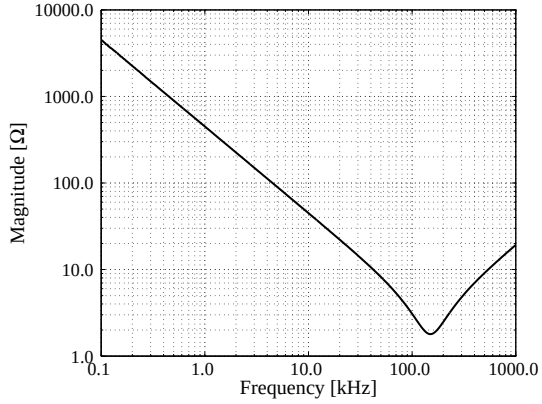
Assuming the polymer of the DEAP film to be incompressible, the capacitance of a sheet of DEAP film can be expressed

$$C_{E0V} = \varepsilon_r \varepsilon_0 \frac{Area}{h_0} = \varepsilon_r \varepsilon_0 \frac{Vol}{h_0^2} \tag{3.1}$$

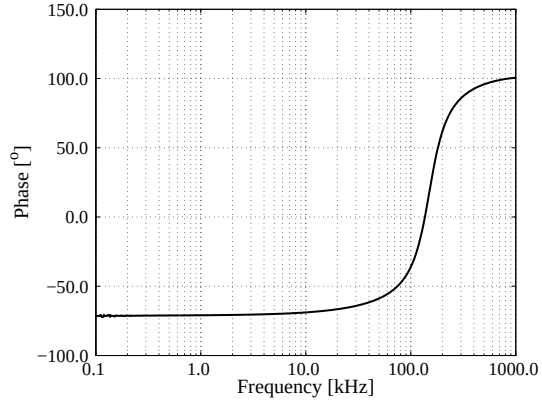
with Vol being the volume of the dielectric material $[m^3]$, $Area$ the electrode surface area $[m^2]$, and h_0 the distance between the electrodes $[m]$, when the film is not deformed.

3.1.2 Mechanical model

The DEAP transducer can be modelled as a second order system consisting of a mass, a spring and a damper. A second order model is needed, because the current version of the DEAP transducer has its first mechanical resonance in the frequency range of 10 – 200 Hz [75, 76]. Figure 3.4 illustrates the mechanical DEAP model. The model is only valid for frequencies below and around the first mechanical resonance.



(a) Magnitude.



(b) Phase.

Figure 3.3: Measured impedance.

The first mechanical resonance is found at the frequency, $f_{Res} = \frac{\sqrt{\frac{k}{m}}}{2\pi}$ with m begin the moving mass [kg], and k the effective spring constant [N/m]. Young's modulus, Y is related to k

$$k = \frac{YA}{l_0} \tag{3.2}$$

A is the cross sectional area of the transducer [m^2], and l_0 the undeformed length of the

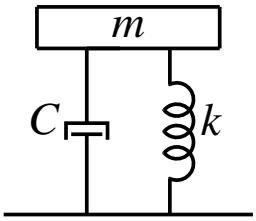


Figure 3.4: Mechanical model.

transducer [m]. This simplified models neglects any geometrical effects due to winding of the DEAP film.

3.1.3 Electrostatics

Like a traditional electrostatic loudspeaker, the electrostatic pressure of the DEAP transducer exhibits squared dependency on the applied voltage [68, 3]

$$\sigma(t) = \varepsilon_0 \varepsilon_r \left(\frac{v_c(t)}{h} \right)^2 \tag{3.3}$$

with ε_0 being the permittivity of vacuum, ε_r, the relative permittivity of the Dielectric Electro (DE) material and h the distance between the electrodes.

Assume a voltage consisting of a DC and an audio component:

$$v_c(t) = v_{Bias} + v_{Audio} cos(2\pi ft) \tag{3.4}$$

It can be shown that:

$$v_c^2(t) = v_{Bias}^2 + v_{Audio}^2 cos^2(2\pi ft) \tag{3.5}$$

$$+2 v_{Bias} v_{Audio} cos(2\pi ft) \tag{3.6}$$

$$v_c^2(t) = v_{Bias}^2 + v_{Audio}^2 \left(\frac{1 + cos(4\pi ft)}{2} \right) \tag{3.7}$$

$$+2 v_{Bias} v_{Audio} cos(2\pi ft) \tag{3.8}$$

From equation (3.8) the THD can be derived:

$$THD = \frac{\frac{v_{Audio}^2}{2}}{2 v_{Bias} v_{Audio}} = \frac{v_{Audio}}{4 v_{Bias}} \tag{3.9}$$

Consequently $v_{Bias} > 25 v_{Audio}$ in order to reach THD below 1%. Proper biasing is thus of key importance, when driving a DEAP transducer. Not only does biasing improve the linearity of the transducer, the electrostatic pressure also rises with the square of the biasing voltage. Typically the applied biasing voltage will be limited by the breakdown voltage of the dielectric material. Figure 3.5 shows the electrostatic pressure as a function of the biasing voltage (equation (1)), while figure 3.6 gives the THD as a function of the biasing voltage with a selection of audio amplitudes imposed.

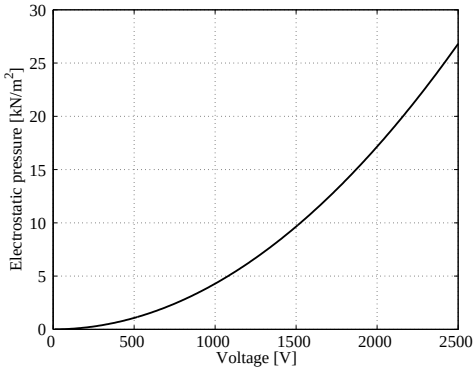


Figure 3.5: Electrostatic pressure of DEAP vs. bias voltage.

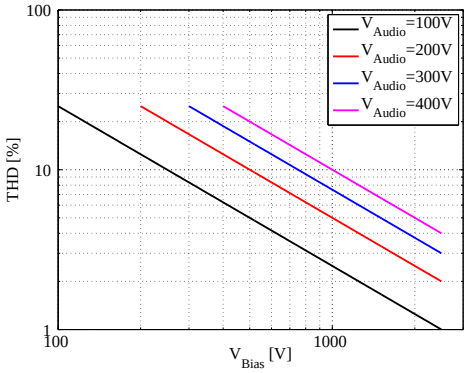


Figure 3.6: Calculated THD of DEAP vs. bias voltage.

3.1.4 Acoustical response

Figure 3.7 shows the measured Sound Pressure Level (SPL) of the push loudspeaker of figure 3.1(b) for a selection of biasing and audio voltages. The first mechanical resonance of the DEAP transducer are found at 200 Hz. Higher order resonances are seen at 700 Hz, 1.3 kHz, 2.3 kHz and 4 kHz. These resonances are very pronounced, and in order to ensure a flat response within the midrange audio band of 100 Hz to 3.5 kHz, significant damping should be applied to the loudspeaker either in the mechanical or acoustical domain. Damping will come at the expense of an increased loss and thus lower efficiency. A redesign of the DEAP transducer used in the loudspeaker is of interest. Higher order finite element analysis will be needed in order to get a complete picture of the frequency response of the DEAP transducer. This is a task for Danfoss Polypower A/S under the ATF project (see figure 1.3), which currently have models capable of modelling only the first mechanical resonance [68]. A better understanding of the resonances in the DEAP transducer, will allow the designer of the transducer and loudspeaker to investigate the possibility of placing these resonances outside the frequency band of interest. At the first mechanical resonance, a peak SPL of 105 dB is achieved. This is a significant advance compared with the SPL of 80 dB reported in [70].

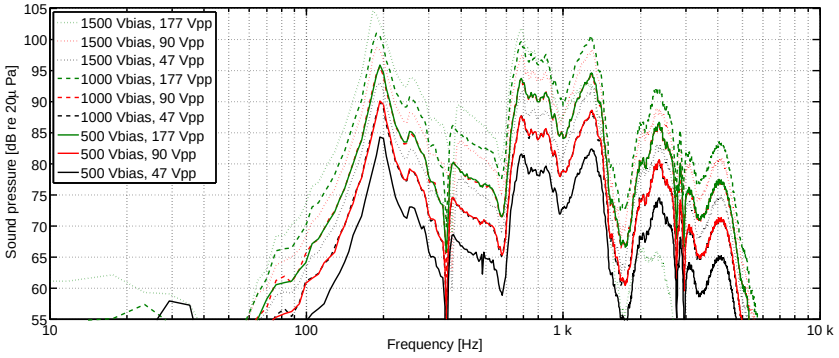


Figure 3.7: Measured Sound Pressure Level (SPL) push loudspeaker.

3.2 Small-signal model

A small-signal model of the DEAP transducer is derived by separating the absolute voltage into a static biasing voltage, V_{Bias}, and a time dependent signal voltage, $v(t)$.

The resulting electrostatic pressure is

$$\sigma(t) = \varepsilon_0 \varepsilon_r \left(\frac{V_{Bias} + v(t)}{h} \right)^2 \tag{3.10}$$

Assuming $V_{Bias} \gg |v(t)|$, the electrical and mechanical relationships of the DEAP transducer can be approximated with a linear small-signal model. A similar approach is found in [70], analysing the condenser microphone.

The capacitance of the DEAP transducer changes with the strain, ε

$$C_E = C_{E0V}(1+\varepsilon)^{k_A} = C_{E0V} \left(\frac{l_0 + l(t)}{d} \right)^{k_A} \tag{3.11}$$

where l_0, is the static length of the transducer in meters [m], d is the undeformed length with no mechanical or electrical biasing applied in meters [m], $l(t)$ is the time dependent length of variation in meters [m] and k_A is a dimensionless constant, specifying the degree of anisotropy. For a prestrain below 10 %, the change in compliance can be neglected [77], hence it can be included as part of the static length.

The electrical and mechanical domain are coupled through the strain. It is possible to define charge and energy balances, which allows for the derivation of the small-signal model. The detailed derivation is presented in [A2]. It is shown, that two linear equations in two unknowns can be formulated to describe the coupling between the electrical and mechanical domain of the DEAP transducer. These are

$$v(\omega) = \frac{i(\omega)}{j\omega C_{E0V}} \left(\frac{l_0}{d} \right)^{-k_A} - \frac{V_{Bias} k_A u(\omega)}{j\omega l_0} \tag{3.12}$$

and

$$f(\omega) = \frac{k_A V_{Bias}}{j\omega l_0} i(\omega) - \frac{u(\omega)}{j\omega C_{M_{Eq}}} \tag{3.13}$$

The frequency dependent voltage, $v(\omega)$ [V], across the DEAP electrodes in equation (3.12), is related to the frequency dependent current, $i(\omega)$ [A], flowing through the DEAP electrodes and the frequency dependent mechanical velocity, $u(\omega)$ [m/s]. In equation (3.13) the frequency dependent force, $f(\omega)$ [N], acting in the compliant direction (see figure 1.2) of the DEAP transducer is related to the frequency dependent electrical current,

$i(\omega)$ [A], runnning through the electrodes and the frequency dependent mechanical velocity, $u(\omega)$ [m/s].

Combining equation (3.12) and 3.13 allows for the establishment of a fully coupled model from the electrical to the mechanical domain of the DEAP transducer. The analogous circuit model is shown in figure 3.8. Two current dependent voltage sources is utilised to express the coupling between the electrical and mechanical domain. In order to simplify the notation, the mechanical domain is modelled as an equivalent compliance, $C_{M_{Eq}}$ [m/N], while the function, $Z_M(\omega)$ [kg], contains the combined mechanical mass and damping. $Z_M(\omega)$ can be extended to include the acoustical domain as well.

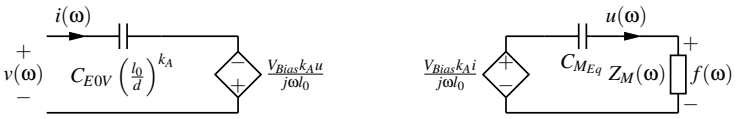


Figure 3.8: DEAP transducer small-signal model.

The transducer under investigation in [A2] is the push-pull loudspeaker of figure 3.1(a) utilising two series connected DEAP cylinders. Figure 3.9 shows the lumped parameter model of the push-pull loudspeaker. This loudspeaker is a device with three electrical terminals. However, for the investigations described in [A2], the bias and signal voltage was only applied to one of the two cylinders. As the coupling between the mechanical and electrical domain is proportional to the bias voltage, the effect of the added, inactive, DEAP element is regarded purely as an altered mass and compliance in the two terminal DEAP model of figure 3.8.

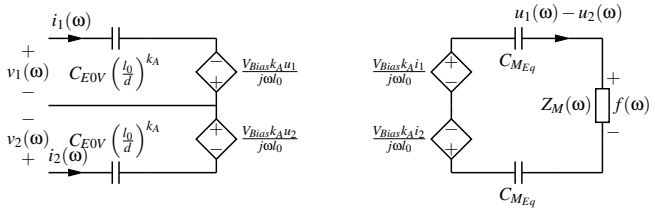


Figure 3.9: Push-pull DEAP transducer small-signal model.

The input impedance of the analogous circuit model in figure 3.8 is

$$Z_{In} = \left(\frac{1}{j\omega C_{E0V}} \left(\frac{l_0}{d} \right)^{-k_A} - \frac{V_{Bias}^2 k_A^2}{(j\omega)^2 l_o^2 \left(Z_M + \frac{1}{j\omega C_{M_{Eq}}} \right)} \right) \tag{3.14}$$

Equation 3.14 consists of two terms: The first is the static capacitance at a certain static strain due to mechanical prestrain and bias voltage. The second term contain the mechanical impedance reflected to the electrical domain through the coupled current dependent voltage sources of figure 3.8. This term will cause the mechanical resonance to appear in the electrical impedance as the bias voltage is increased. A similar result is found in [35], analysing the output impedance of the condenser microphone. The small-signal model does not include the effect of altered geometries nor complex vibrational modes. Hence, the model cannot be relied on above the first mechanical resonance, where such phenomenons are expected to occur.

In order to characterise the DEAP transducer, its input impedance is measured with a biasing source connected. The measuring setup of [A2] is shown in figure 3.10. A frequency response analyzer, AP300, from Ridley Engineering connected to an isolation transformer couples the test signal to the DEAP transducer. A Matsusada AU-5R60 high voltage supply ensures the bias voltage, with the $R_{Bias}C_{Bias}$ circuit providing a low impedance return path for the test signal. For the measurements $C_{Bias} = 10C_{E0V}$, $R_{Bias} = 1M\Omega$ and $R_{Sense} = 10\Omega$. A 1/200 differential probe was used to measure the voltage $v_{Out} + v_{Sense}$. An alternative measuring setup is proposed in [78] using a capacitive balanced bridge to measure the motional current of the DEAP transducer. The motional current is defined as the current trough the controlled voltage source at the electrical side of figure 3.8 and figure 3.9. This measuring setup is proposed by Peter Walker for characterisation of the electrostatic loudspeaker [78]. The setup relies on a capacitive balanced bridge, and is highly sensitive to components tolerances, making it unsuitable for most practical applications. Accordingly, this approach is disregarded.

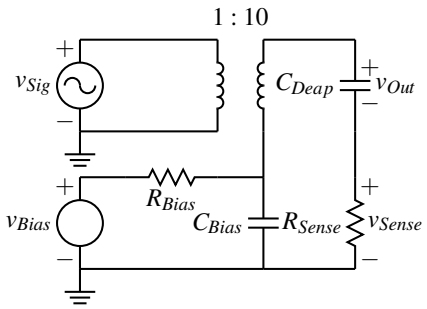


Figure 3.10: Setup for measuring impedance under different bias voltages.

Measurements are presented on the push-pull DEAP transducer loudspeaker in figure 3.1(a). The push-pull loudspeaker is characterised using a 5 % pre-strain. During the measurements the bottom DEAP element is left as an open circuit. It is assumed, that symmetry applies and it is not within the scope of [A2] to investigate any mismatch in the elements. Figure 3.11(a) gives the measured impedance for a selection of bias voltages.

	Designator	Value
Biasing voltage	V_{Bias}	0 –2.4 kV
Constant	k_A	2
Young's modulus	Y	2 MPa
Relative permittivity	ε_r	3
Vacuum permittivity	ε_0	8.854 $\frac{pF}{m}$
Average film thickness	h_0	40 μm
Length of un-rolled DEAP	b	3 m
Active height of DEAP cylinder	d	2 cm
Compliance	$C_{M_{Eq}}$	83.3 $\frac{\mu m}{N}$
Capacitance at 5 % pre-strain	C_{E0V}	58.3 nF
Moving mass	L_M	15 g
Mechnical damping resistance	R_M	20 $\frac{Ns}{m}$

Table 3.1: Parameters of the push-pull loudspeaker

Notice that the input impedance is almost exclusively capacitive, and that the log-log plot only reveals the small change in the static capacitance. In order to make the effects of the bias voltage visible, the measured impedance at a given biasing voltage is normalized with the unbiased measured impedance, as shown in figure 3.11(b). Plotting the results on a linear y-axis shows, that the biasing voltage does indeed influence the impedance of the DEAP transducer. According to equation 3.11 the static capacitance should increase with the strain of the material. This is seen in figure 3.11(b), where the static capacitance dominates the impedance from 100 Hz and below. Another key observation is the mechanical resonances. The push-pull DEAP loudspeaker has its first mechanical resonance at 160 Hz. As the biasing voltage is increased this resonance peak becomes increasingly visible in the electrical domain. This is in accordance with equation (3.14).

Figure 3.11(b) shows significant noise at frequencies below 100 Hz. This is due to the limited bandwidth used for the measurements (10 Hz), and poor signal to noise ratio at these very low currents. Better signal to noise ratio can be achieved by using a higher value sense resistance. This is however at the expense of the bandwidth and losses in the sense resistance of the measuring setup.

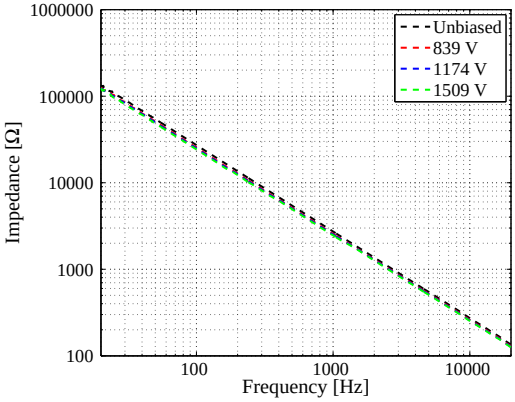
The calculated normalized impedances using equation (3.14) are plotted in figure 3.11(b) for the parameters of Table 3.1. It is seen in figure 3.11(b), that the model predicts the change in static impedance within 10 %, while taken into account the first resonance of the DEAP structure. Note that parameter tolerances of DEAP transducers is not a well-documented area, however [75] reports of a 4 % spread in resonance frequency over 3 samples from the same production run. Especially the estimated moving or active mass

is a rough estimate, assuming that half of the DEAP mass is moving [75]. Finite element analysis can be used to determine the actual moving mass. The model suggested in [A2], relies on Hooke's law for modeling the compliance of the DEAP transducer [68]. Greater accuracy could be achieved by instead using the Mooney-Rivling equation for the compliance of the DEAP actuator [79]. It is proposed in [76] to model a tubular DEAP transducer using the modified Mooney-Rivlin equation. The modification is achieved by introducing a hardening factor taken into account the influence of the electrode. Also the coupling between the acoustical and mechanical domains can be included. This subject is, however well documented in the literature [35], and the influence is expected to be negligible due to a large box in which the DEAP transducer was mounted, ensuring the compliance of the system to be dominated by the transducer.

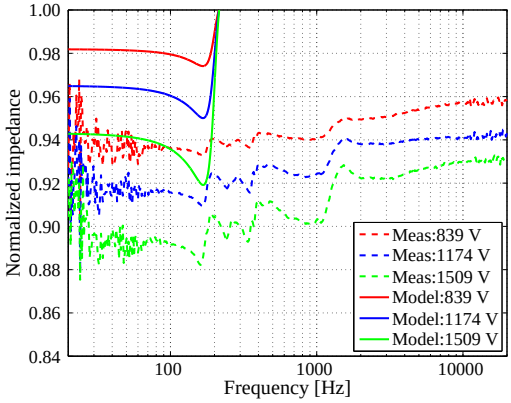
The complexity of the model can be increased in the pursuit of greater accuracy in numerous ways. Nevertheless [A2] documents, that the DEAP transducers based loudspeaker is to be considered as an almost exclusively capacitive load. However, as the material properties of the DEAP improves, and the thickness of the dielectric material is reduced, the model should be revisited with the new electrical and mechanical parameters, in order to verify that this conclusion is still valid.

3.3 Conclusion

The large- and small-signal model of the DEAP transducer is presented and analyzed. A peak SPL of 105 dB is achieved, representing an advance comparing with the 80 dB reported in [70]. Impedance measurements are used to characterise the DEAP transducer. A significant number of mechanical resonances is shown to be present within the considered audio band. Research into damping or moving these resonances outside the audio band is needed. If the DEAP technology is to success for the application of audio, the SPL frequency response should be flat within 3 dB or less.



(a) Impedance.



(b) Normalized impedance.

Figure 3.11: Impedance measurements of push-pull loudspeaker.

CHAPTER 4

2-Level modulators

The motivation for researching class D amplifiers based on the half-bridge power stage was divided into:

- Investigation of linearity and efficiency. This is the subject of [A1], [A3], [A4] and [A8].
- Design and implementation of second order output filter control scheme. This is the subject of [A1], [A3] and [A4].
- Design and implementation of fourth order output filter control scheme. This is the subject of [A6].

4.1 Losses and pulse timing errors

4.1.1 Switch realisation

Switches in power electronics applications are implemented using the MOSFET (Metal-oxide-semiconductor field-effect transistor), BJT (Bipolar junction transistor), thyristor or IGBT (Insulated Gate Bipolar Transistor). The majority carrier based MOSFET is traditional selected for class D audio amplifiers due to their superior switching speeds compared with the minority carrier based (IGBT, BJT and thyristor).

MOSFETs are found with voltage ratings of 4 kV and below [80]. A threshold around the 600 – 1200 V limit is observed, as very few commercial applications need higher

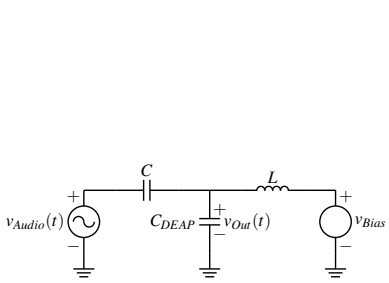
operating voltages. A selection of SiC MOSFETs with the voltage rating of 1200 V are starting to emerge. With the target of ensuring the minimum voltage stress of the MOSFETs, it is proposed to separate the audio and biasing component of the drive signal into separate sources. This will allow for a single ended amplifier to be designed with MOSFETs having a voltage rating only supporting that of the needed audio component, while an external high voltage source ensures the biasing.

A number of ways for implementing the separate sources configuration are depicted in figure 4.1. Figure 4.1(a) and 4.1(b) illustrate drive configurations for a two terminal push DEAP loudspeaker like the one shown in figure 3.1(b) figure 3.1(c), while figure 4.1(c) and 4.1(d) represents push-pull configurations for the loudspeaker of figure 3.1(a). Notice how figure 4.1(c) corresponds to the traditional way of driving an electrostatic loudspeaker [3] typically implemented using an audio-transformer. The main difference between 4.1(a) and the rest is, that a high voltage DC blocking capacitor together with a coupling inductor is needed. Especially the DC blocking capacitor is troublesome, as it must be rated for the full bias voltage, and must be significant larger than the DEAP capacitance in order to provide a low impedance path for audio component. In the configurations of figure 4.1(b), 4.1(c) and 4.1(d) the output impedance of the biasing source is very important, as the audio should be presented to a low impedance path, which does not add THD.

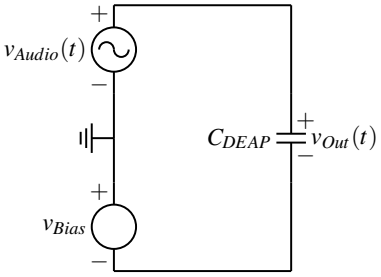
Proposed implementations of class D amplifiers for capacitive transducers needing a biasing voltage are shown in figure 4.2 and figure 4.3. In both cases the two terminal push DEAP transducer is assumed. The concepts can be extended to the three terminal push-pull DEAP transducer if needed.

Both figure 4.2 and figure 4.3 relies on a DC-link between the class D amplifiers and the power supply of the class D amplifier. In figure 4.2 a passive rectifier is used for the biasing, while an active rectifier is used in figure 4.3. The main difference between the two implementations of the biasing source is the output impedance. For the passive rectifier, the only way of ensure that the output impedance of the biasing source stays below the impedance of the DEAP capacitance, C_{DEAP}, is to choose $C > C_{DEAP}$. The output impedance of the active rectifier is the parallel connection of L_2 and C_2, with the option of suppressing the output impedance by the loop-gain of the control-loop of the biasing source [63]. Having an active rectifier biasing source with audio band-width will however undermine the concept of separated sources, as the biasing source itself becomes a class D audio amplifier.

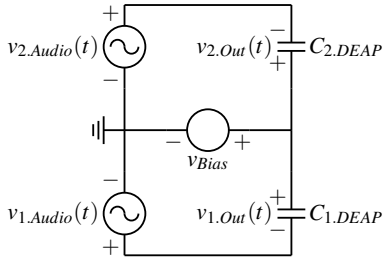
Figure 4.4 shows a picture of a prototype amplifier, including the biasing circuit needed to drive the push-pull DEAP loudspeaker of figure 3.1(a). The amplifier of the picture runs in open-loop with a fourth-order output filter. In order to ensure biasing, two *RC*-circuits is utilises together with two Matsusada AU-5R60 high voltage supplies. The case of passive biasing is thus illustrated in this implementation example. More than one third of the space on the PCB is occupied with the high voltage biasing capacitance.



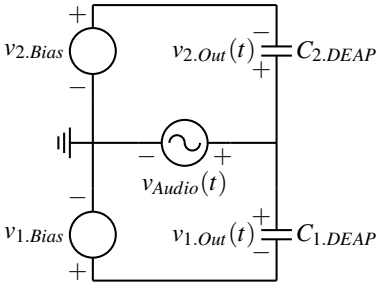
(a) DC-blocking



(b) Single stage or stacking configuration.



(c) Push-pull with dual audio stage.



(d) Push-pull with single audio stage.

Figure 4.1: Biasing configurations.

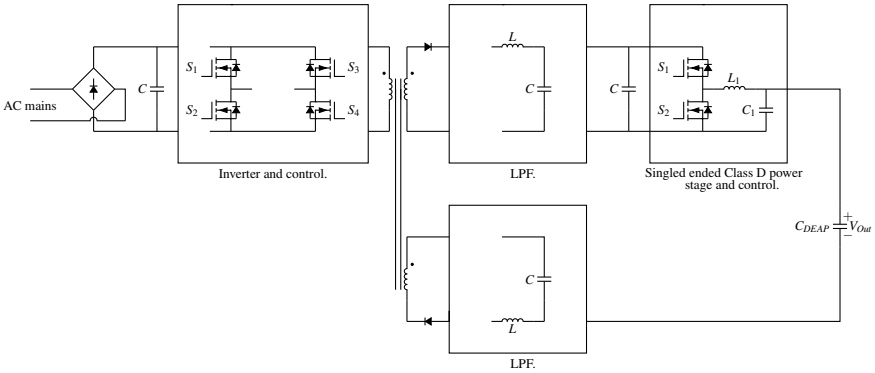


Figure 4.2: Block diagram of mains operated class D amplifier for DEAP transducers with passive biasing source.

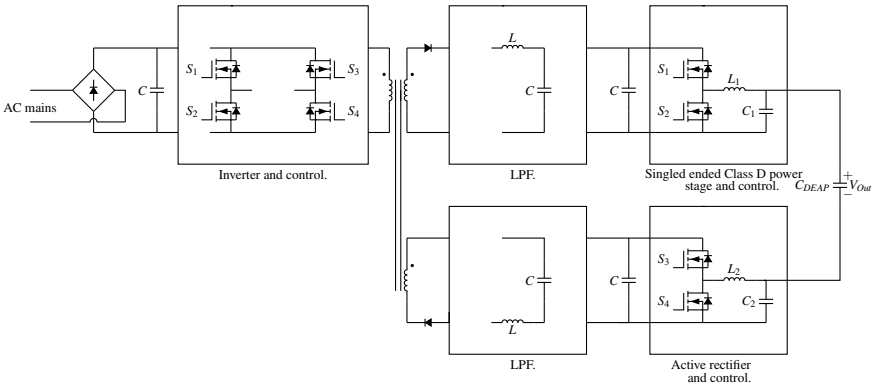


Figure 4.3: Block diagram of mains operated class D amplifier for DEAP transducers with active biasing source.

Besides lowering the power density, the biasing circuit contributes significantly to the cost of the amplifier. Just the capacitance of figure 4.4 cost 8 times 2.59 $ corresponding to 121.84 danish kroner[1] [81]. A cost that the traditional class D amplifier driving the electrodynamic transducer does not need to bear. Another concern with respect to the cost, is that of the high voltage MOSFETs. A state-of-the-art class D amplifier driving the electrodynamic transducer and producing a peak output power of 100 W, can be build with IRF6645 Direct-FETs [18]. The cost of a single IRF6645 is 19.9 danish kroner [82]. The amplifier of figure 4.4 uses the 800 V SPA08N80C3 MOSFET of INFINEON at a cost of 26.35 danish kroner for a single MOSFET [83]. If higher volt-

[1] http://www.valutakurser.dk, 27/10-14

age MOSFETs are needed, in order to increase the amplitude of the audio component, it will be at the expense of an increased cost. The 1500 V, STW4N150 MOSFET of STMicroelectronics is 5.78 € corresponding to 43.03 danish kroner[2] [84]. Competing on the power density and cost is thus not possible using the half-bridge power stage for the class D amplifier of the DEAP transducer. The main driver of the cost being the additional circuity needed for biasing. Building an active biasing source with audio band-width could be take into account as a doubling of the system-cost, depending on the operational voltages needed.

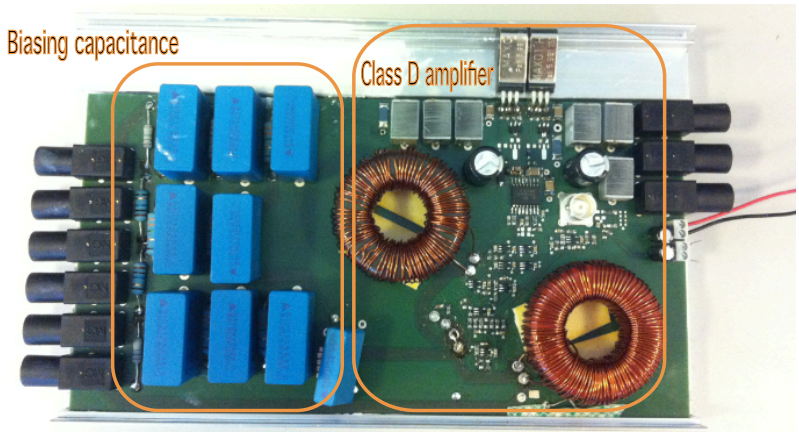


Figure 4.4: Picture of prototype amplifier for the push-pull DEAP loudspeaker of figure 4.4.

4.1.2 Losses

The propose of this section is to investigate the losses in class D audio amplifiers for DEAP transducers. A calculation example is presented using the parameters of the second order output filter prototype amplifier, presented later in this chapter. Losses in class D audio amplifiers driving the electrodynamic transducer is investigated in [25, 26]. The half-bridge power stage is shown in figure 4.5. Notice, that the inductor current equals the current through C_{DEAP} ($i_L(t) = i_{DEAP}(t)$), because the parallel resistance of the DEAP transducer has a value of 1 MΩ or above [68]. With a capacitive load of $C_{DEAP} = 100nF$, the cutoff frequency of the parallel connection between C_{DEAP} and the DEAP transducer parallel resistance, becomes $\frac{1}{2\pi 1M\Omega 100nF} = 1.59$ Hz. The impedance of the DEAP transducer, is thus capacitive even at the lowest frequency

[2] http://www.valutakurser.dk, 27/10-14

of the audio band, 20 Hz. The peak ripple current is [63]

$$\Delta i_L(D(t)) = 2V_{CC}\frac{D(t)-D(t)^2}{f_{Sw}L_{Out}} \tag{4.1}$$

The current $i_{DEAP}(t)$ is a superposition of the ripple current and the sinusoidal reference or audio current ($i_{Ref}(t)$). An expression for the envelope of $i_{DEAP}(t)$ can be formulated

$$i_{DEAP_{Env}}(t) \quad = \quad \pm\Delta i_L(D(t)) + i_{Ref}(t) \tag{4.2}$$

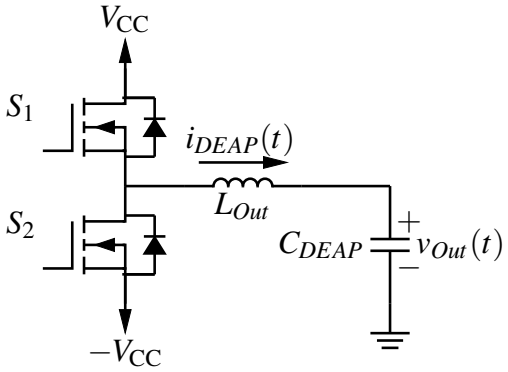


Figure 4.5: Half-bridge class D amplifier with DEAP load.

The Root Mean Square (RMS) of equation (4.1) can be expressed as a function of the modulation index, M. Using the relation $D(t) = \frac{1}{2}(Msin(2\pi f_{Ref}t)+1)$ it can be shown that [23]

$$\Delta i_{L_{RMS}}(M) = \frac{V_{CC}}{4Lf_{Sw}}\sqrt{\frac{1-M^2}{3}+\frac{M^4}{8}} \tag{4.3}$$

The RMS value of the reference current is defined as

$$i_{Ref_{RMS}}(M) = \frac{V_{CC}M}{\sqrt{2}}2\pi f_{Ref}C_{DEAP} \tag{4.4}$$

The RMS value of the total reference and ripple current is calculated as

$$i_{DEAP_{RMS}}(M) = \sqrt{\Delta i_{L_{RMS}}(M)^2 + i_{Ref_{RMS}}(M)^2} \tag{4.5}$$

DEAP loss

The DEAP transducer is modelled as a capacitor with a series resistance, neglecting dielectric losses and the parallel resistance. Denoting the DEAP series resistance, R_S, yields

$$P_{DEAP} = i_{DEAP_{RMS}}(M)^2 R_S \tag{4.6}$$

Magnetic loss

The magnetic loss is divided into conduction and ferrite loss. Conduction losses are defined as

$$P_{Cu} = i_{DEAP_{RMS}}(M)^2 R_{Cu} \tag{4.7}$$

with

$$R_{Cu} = \frac{\rho N l_T}{A_{Wire}} \tag{4.8}$$

N is the number of turns, l_T the average length of a turn [m], A_{Wire} the wire cross-sectional area [m^2] and ρ the resistivity of copper, 16.8 $n\Omega m$. A single layer winding scheme on a toroidal core is considered.

Steinmetz equation are used to estimate the ferrite loss

$$P_{Fe} = V_{Core} k_{Fe} \left(\left(\frac{f_{Ref}}{f_0} \right)^{\alpha} \left(\frac{B(i_{Ref})}{B_0} \right)^{\beta} + \left(\frac{f_{Sw}}{f_0} \right)^{\alpha} \left(\frac{B(\Delta i_L(M))}{B_0} \right)^{\beta} \right) \tag{4.9}$$

Greater accuracy can be achieved by use of the improved Steinmetz equation [85]. The ferrite loss can be expressed as a function of the modulation index [86, 87]. However a worst case approximation is found using the peak ripple current at idle [23].

Semiconductor losses

The semiconductor losses are divided into the conduction and switching loss. The conductions loss caused by the MOSFET on resistance, $R_{DS_{On}}$, is

$$P_{DS_{On}} = R_{DS_{On}} i_{DEAP_{RMS}}(M)^2 \tag{4.10}$$

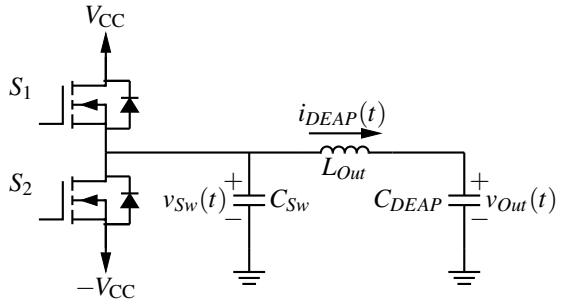


Figure 4.6: Half-bridge class D amplifier with equivalent switching node capacitance.

The switching loss can be approximated by [88]

$$P_{Sw} = \begin{cases} 2 f_{Sw} C_{Sw} V_{Sw}^2 & \hat{I}_{Ref}(M) \leq \Delta i_L(M) \\ f_{Sw} V_{CC} \tau(I_{Ref}) \frac{\hat{I}_{Ref}}{\pi} + 2 f_{Sw} C_{Sw} V_{Sw}^2 & \hat{I}_{Ref}(M) > \Delta i_L(M) \end{cases} \tag{4.11}$$

with

$$\tau(I_{Ref}) = R_G Q_{GD} \left(\frac{1}{v_{GS,th} + \frac{I_{Ref}}{g}} + \frac{1}{V_G - v_{GS,th} - \frac{I_{Ref}}{g}} \right) \tag{4.12}$$

$$+ R_G C_{ISS} \ln \left(\frac{v_{GS,th} + \frac{I_{Ref}}{g}}{v_{GS,th}} \frac{V_G - v_{GS,th}}{V_G - v_{GS,th} - \frac{I_{Ref}}{g}} \right) \tag{4.13}$$

C_{Sw} is the parallel connection of two times the MOSFETs drain-source capacitance, the heat-sink capacitance and the series connection of the output filter inter-winding capacitance together with C_{DEAP}. The MOSFETs drain-source capacitance is a nonlinear function of the drain-source voltage [63].

	Designator	Value
Drain-source on resistance	$R_{DS_{On}}$	650 mΩ
Drain-source capacitance (at 500 V)	C_{DS}	20 pF
Number of inductor windings	N	92
DC resistance of output filter inductor	R_S	404 mΩ
Switching frequency	f_{Sw}	300 kHz
Output filter inductance	L_{Out}	200 uH
DEAP Capacitance	C_{DEAP}	100 nF
Supply voltage	V_{CC}	± 300 V

Table 4.1: Parameters key to the loss analysis.

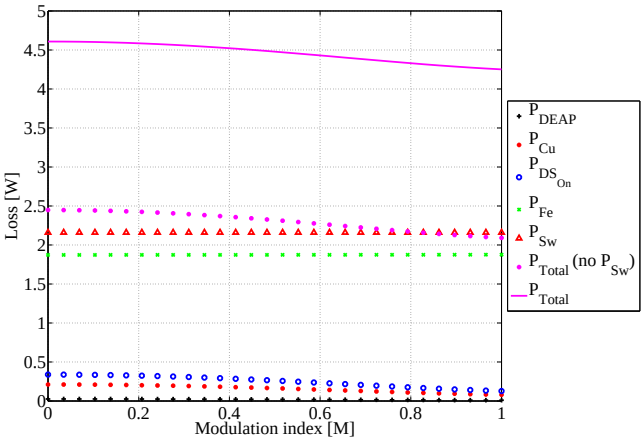


Figure 4.7: Calculated losses of the half-bridge class D amplifier for the reference frequency of 1 kHz.

4.1.3 Efficiency

Figure 4.7 shows the calculated distribution of losses in the half-bridge class D amplifier using the parameters of table 4.1 and assuming the SPA08N80C3 MOSFETs of Infineon [89]. The calculated efficiency is shown in figure 4.8 using the definition of equation (2.5). Results are plotted for the reference frequencies of 100 Hz, 1 kHz and 3.5 kHz. The efficiency is calculated with and without the switching loss. At the reference frequency of 100 Hz, the efficiency stays below 40 %. The is a consequence of equation (2.5). A frequency depended, reactive output power is considered. At low reference frequencies the reactive output power, becomes comparable with the real power loss of the amplifier. The calculated efficiency, with the switching loss excluded,

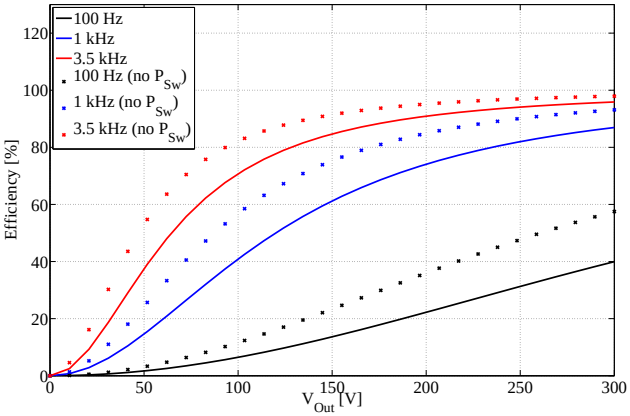


Figure 4.8: Calculated efficiency of the half-bridge class D amplifier.

of figure 4.8, motivates the investigation of soft switching or Zero Voltage Switching (ZVS). Besides the improved efficiency, ZVS features two additional benefits. The noise-floor is improved, due to the lack of hard switching, and dv/dt induced turn on of the MOSFETs is eliminated. Another advantage of ZVS is the fact, that the RC-snubbers typically used in half- and full-bridge class D power stages can be eliminated [25, 26]. A disadvantage of ZVS is, that the MOSFETs body diode starts conducting. The linearity of the MOSFET body diode thus becomes a concern.

ZVS is ensured by allowing the inductor current to charge and discharge the equivalent switching node capacitance, C_{Sw}, before performing a switching transition. As a consequence, the term $2f_{Sw}C_{Sw}V_{Sw}^2$ of equation (4.11), can be eliminated or minimised depending on the ability of the amplifier to ZVS [63]. Assuming the dead-time required to achieve ZVS is significant smaller than the switching period, the output filter inductor can be considered an ideal constant current source

$$v_{Sw} = \frac{1}{C_{Sw}} \int_0^{t_{Dead}} i_{DEAP}(D)\,\mathrm{d}t \tag{4.14}$$

$$= \frac{t_{Dead} i_{DEAP}(D)}{C_{Sw}} \tag{4.15}$$

The quasi-square wave ZVS buck converter is analyzed in [63], and ZVS is guaranteed at idle (50 % duty cycle or M=0) , if the switches are operated with sufficient dead-time. If $v_{Sw} = 2V_{CC}$, the dead-time, t_{Dead}, can be calculated as

$$t_{Dead} = \frac{2V_{CC}C_{DEAP}}{i_{DEAP}(D)} \tag{4.16}$$

4.1.4 Dead-time distortion

Several publications have analysed the influence of pulse-timing errors on THD [90, 91, 88, 92]. These are traditional divided into the categories:

- Dead-time distortion.
- Finite switching speed.
- Conduction state errors.

Amplitude modulation errors through power supply pumping is another source of THD, this subject is covered in [25].

When operating the power stage at ZVS, the dead-time distortion becomes a key concern. It is shown in [88], that dead-time distortion is a function of the ratio between reference and ripple current. This section analyzes dead-time distortion for a class D amplifier driving a capacitive load. Voltage mode control is assumed, meaning that the output current no longer can be considered constant with respect to frequency. This is unlike the case of driving an electrodynamic loudspeaker, where the load typically is assumed being resistive, and thus the output current does not change with frequency. Let the THD arising from dead-time distortion being defined as [88]

$$THD_d(M,\alpha_d,\alpha_I) = \frac{\Delta(\alpha_I)\sqrt{\sum_{i=2}^{N_{Max}}\left[2\alpha_d\frac{sin(i\frac{\pi}{2})}{i\frac{\pi}{2}}\right]^2}}{M-\alpha_d\frac{4}{\pi}\Delta(\alpha_I)}$$

where the dead-time delay factor is the ratio of the dead-time to the period of the switching frequency

$$\alpha_d = \frac{t_{Dead}}{T_{sw}} \tag{4.17}$$

and the ripple current factor

$$\alpha_I = \frac{\Delta i_L(M)}{i_{Ref}(M)} \tag{4.18}$$

The ripple current factor is the amplitude of the ripple current divided by the reference current. Both being functions of the modulation index.

Using the ripple current factor of equation 4.18, it is defined that

$$\Delta(\alpha_I) = \begin{cases} 0 & i_{Ref}(M) \leq \Delta i_L(M) \\ \frac{\frac{\pi}{2} - arcsin(\alpha_I)}{\frac{\pi}{2}} & i_{Ref}(M) > \Delta i_L(M) \end{cases} \tag{4.19}$$

Similar results can be found in [93].

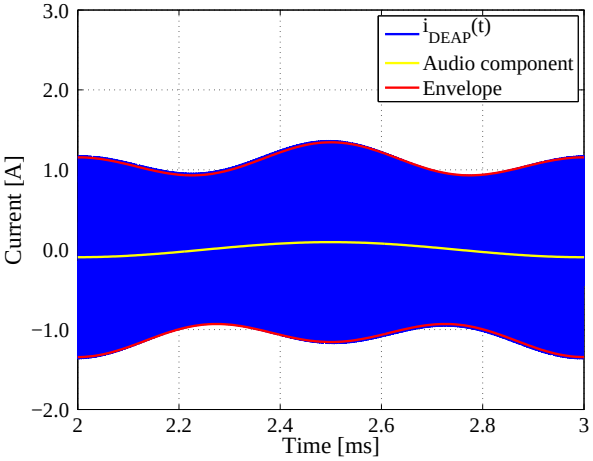
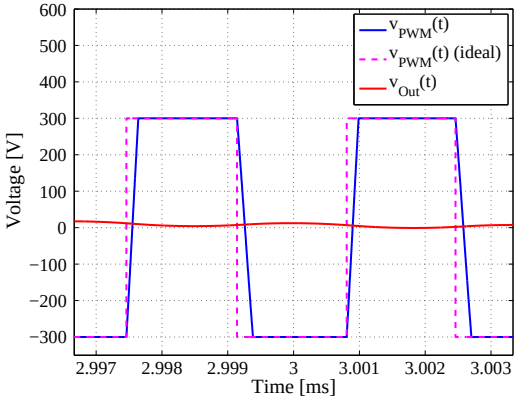


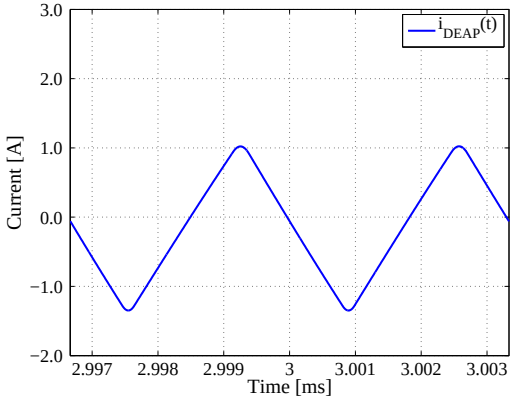
Figure 4.9: Simulated time domain waveforms of the ripple current, the reference current and the envelop of the DEAP current.

Simulated time domain waveforms of the ripple current, the reference current and the envelop of the DEAP current is shown in figure 4.9 for the parameters of table 4.1. A modulation of 0.5 and reference frequency of 1 kHz is utilised. It is observed, that $i_{Ref}(M) \leq \Delta i_L(M)$. Equation (4.17) thus predict zero dead-distortion, and its necessary to investigate, if this prediction is true. The simulation strategy described in [A8] is used to perform the investigation together with the parameters of table 4.1.

Figure 4.10 shows the switching node and output voltage at a modulation index of 0 for $t_{Dead} = 100$ ns and $C_{Sw} = 100$ pF. The ideal switching node is presented together with the switching node voltage at a finite dead-time sufficient to achieve ZVS at idle (M = 0). An average pulse error of zero is observed. Figure 4.11 shows the switching node and output voltage at a modulation index of 0.5. Comparing the ideal switching node voltage and the ZVS switching node voltage a none zero average pulse error is observed. Figure 4.12 and 4.13 shows the simulated spectrum of the output voltage assuming a reference frequency of 1 kHz and modulation index of 0.8. In figure 4.12 $C_{Sw} = 100$ pF and $t_{Dead} = 100$ ns, while $C_{Sw} = 200$ pF and $t_{Dead} = 200$ ns in figure

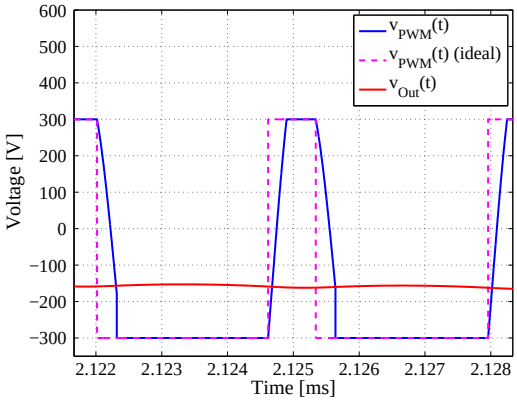


(a) Switching node (ideal and ZVS) and output voltage.

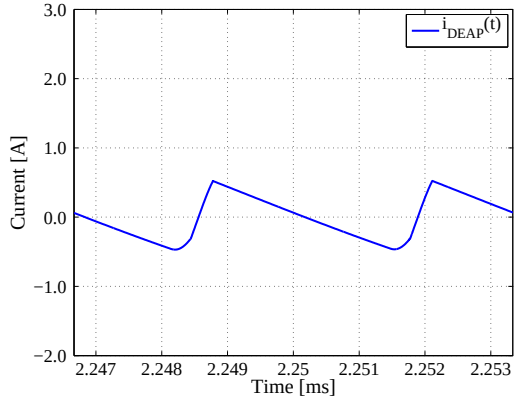


(b) DEAP current.

Figure 4.10: Time domain waveforms at idle (M = 0).



(a) Switching node (ideal and ZVS) and output voltage.



(b) DEAP current.

Figure 4.11: Time domain waveforms at M = 0.5.

4.13. THD of 0.05 % and 0.12 % is observed for the two simulations. Equation (4.17) does not take into account the trapezoidal shape of the switching node voltage, and thus the dead-time distortion under ZVS is not accounted for.

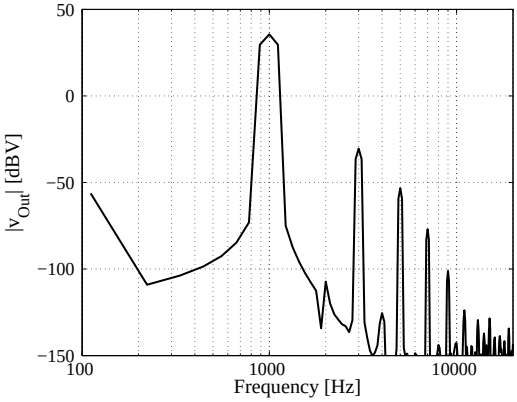


Figure 4.12: Spectrum of output voltage ($C_{Sw} = 100$ pF and $t_{Dead} = 100$ ns). THD = 0.05 %.

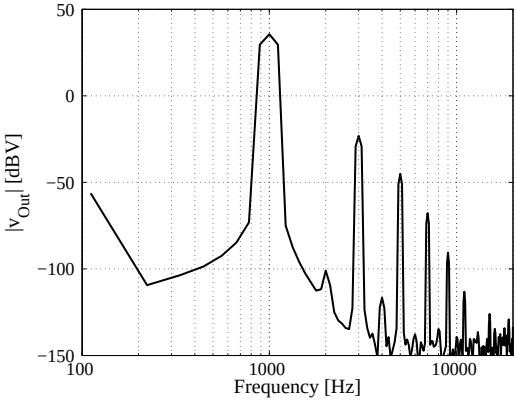


Figure 4.13: Spectrum of output voltage ($C_{Sw} = 200$ pF and $t_{Dead} = 200$ ns). THD = 0.12 %.

In order to give a better understanding of the dead-time distortion under ZVS, parametric sweeps is performed using Matlab. Figure 4.14 shows the simulated THD for three different sets of C_{Sw} and t_{Dead} assuming a reference frequency of 1 kHz. The dead-time distortion can not be ignored under ZVS. In order to minimise the distortion

arising from the t_{Dead} needed for ZVS, MOSFETs with low drain-source capacitance should be selected. Also the interwinding capacitance of the output filter inductor, combined with the PCB layout, is critical in order to ensure the lowest possible switching node capacitance.

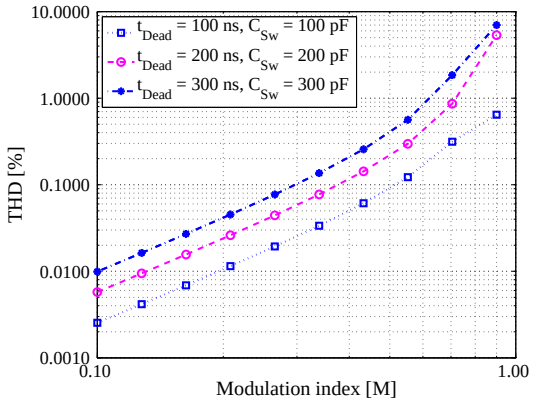
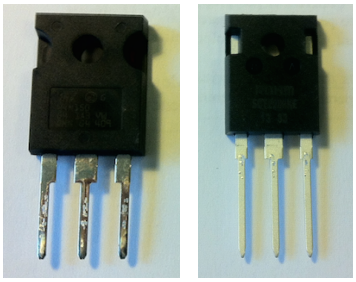


Figure 4.14: Simulated THD at a reference frequency of 1 kHz.

4.1.5 SiC MOSFETs

[A8] investigates high voltage Si and SiC MOSFETs for the application of audio amplifiers. Experimental measurements are performed on a 100 Var self-oscillating class D audio amplifier build around a half-bridge power stage. The hysteresis based bandpass current mode control (BPCM) scheme presented later in this chapter is utilised. Two identical amplifiers are constructed, one using Si MOSFETs STW4N150 [94], while the other is using the SiC MOSFETs SCT2450KEC [95]. Figure 4.15 shows the two test subjects. The STW4N150 MOSFETs were driven by a 18 V gate-source voltage, while the SCT2450KEC MOSFETs were driven by a gate-driver having a supply voltage of -4.5 V to 22.5 V with respect to its source voltage. Measurements are preformed at a power supply voltage of plus/minus 500 V. The idle switching frequency is kept constant for both amplifiers at 100 kHz.

Measured THD+N is plotted in figure 4.16 and 4.17 for the two test subjects of SCT2450KEC and STW4N150 as function of the peak output voltage. Assuming voltage mode control the reactive output power will change with reference frequency, making it unsuitable to plot THD+N as function of power. Measurements are given for the reference frequencies of 100 Hz and 1 kHz. A midrange application is considered (100 Hz – 3.5 kHz).



(a) STW4N150. (b) SCT2450KEC.

Figure 4.15: Test subjects.

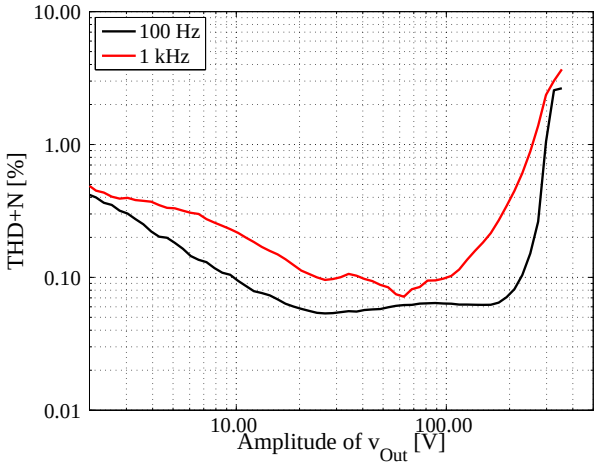


Figure 4.16: Measured THD+N for the STW4N150 Si MOSFET.

From figure 4.16 and 4.17 two key observations can be made. The noise-floor is significant worse for the SiC MOSFETs, than that of the Si MOSFETs. In the region where THD dominates (high modulation index) the two types of MOSFETs perform identically. Both figure 4.16 and 4.17 show THD+N of 0.3 % at a peak output voltage of 200 V and frequency of 1 kHz. ZVS operation at idle is utilised for both MOSFETs. Note, that C_{Sw} is a function of not only the MOSFETs drain-source capacitance, but also the series connection of the output inductor interwinding capacitance and output capacitance, together with the heat-sink capacitance. Especially the output filter interwinding capacitance contributes significantly to C_{Sw}, causing C_{Sw} to be considered identical for both MOSFETs. Consequently the distortion, arising from the dead-time needed to

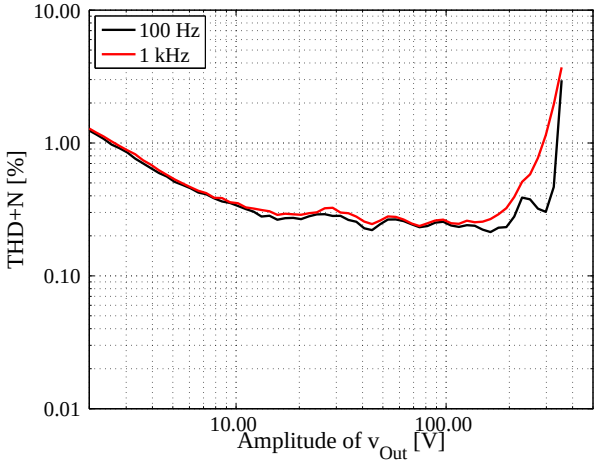


Figure 4.17: Measured THD+N for the SCT2450KEC SiC MOSFET.

ZVS, must be identical. It is assumed, that the optimal dead-time is selected. The body diode characteristics of the MOSFETs is not identical, and will cause the THD+N to differ.

4.2 Second order output filter

Assuming a purely capacitive load, the LC output filter will be undamped. A fundamental choice between active and passive damping has to be made. Passive damping can be implemented using dissipative components like resistors, while active damping can be achieved through the control scheme. In order to estimated the energy lost in a system based on passive damping of the LC output filter, the definition of the quality factor must be remembered

$$Q = 2\pi f \frac{U_{Stored}}{P_{Loss}} \tag{4.20}$$

With U_{Stored} being the energy stored in joules [J] and P_{Loss}, the loss of power in watts [W].

The energy in a capacitor is $\frac{1}{2}CV^2$, and critical damping is achieved if Q = 1/2. During

a step from V_1 to V_2 the energy contained in the oscillation can be calculated as

$$U_{Stored} = \frac{1}{2}C|{V_1}^2 - {V_2}^2| \tag{4.21}$$

The loss of power during a step assuming critical damping is

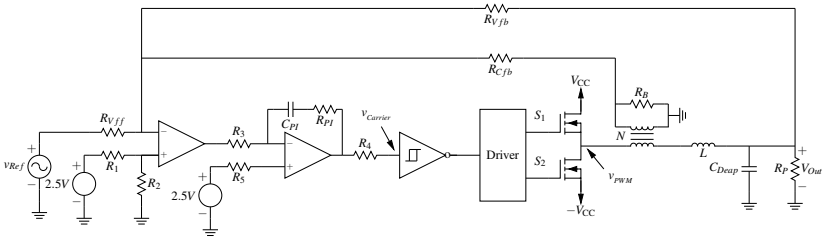
$$P_{Loss} = 4\pi f U_{Stored} \tag{4.22}$$
$$= 2\pi C f|{V_1}^2 - {V_2}^2| \tag{4.23}$$

Assuming a 1 kHz square output stepping between 100 V and 300 V together with a capacitor of 100 nF, the power dissipated will be 50.3 W. Not only does such a power dissipation call of a sizeable power resistance. The converter efficiency will also suffer significantly as peak power levels of 100-200 Var are considered. Therefore, passive damping is not a suitable choice for the considered application of class D amplifiers for DEAP transducers.

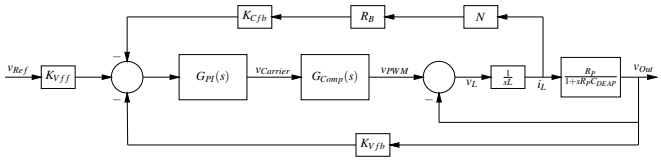
The BPCM (Bandpass current mode) control scheme for buck type power stages is proposed in [96] for the application of fixed frequency amplifiers, while the concept has been extended to self-oscillating class D audio amplifiers in [18, 26, 97, 98, 99]. The big advantage of such control schemes is the fact, that stability is maintained, even when no load is connected to the amplifier. As a consequence the zobel network used to damp the high Q of an unloaded amplifier can be eliminated [18]. Active damping is essentially what the BPCM scheme ensures by letting the output filter inductor act as a current source around the resonance frequency of the output filter. Implementation of the BPCM scheme is achieved by either direct measurement or estimation of the inductor current [100, 69]. For this application the inductor current is measured using a current sense transformer. Accordingly an isolated feedback signal with enough bandwidth to handle the switching frequency is obtained. Figure 4.18(a) shows a schematic of the class D amplifier with BPCM control scheme, while figure 4.18(b) gives the small-signal model of the amplifier. Adding complex poles to the control loop of the amplifier is suggested in [22, 16, 17] as a way of optimising the DC-transfer function over duty cycle of the self-oscillating amplifier. This is an alternative way to implement active damping, however no scientific articles are found using the approach for the propose of damping.

A prototype amplifier has been constructed. The amplifier operates from $\pm$ 300 V delivering a maximum power of 125 Var to a 100 nF capacitive load. Table 4.2 shows the key design parameters of the prototype amplifier.

Figure 5.5 shows the reference, switching node and output voltages, when operating with a reference frequency of 1 kHz and peak output voltage of 150 V (modulation



(a) Schematic with single-supply control circuitry.



(b) Small-signal model.

Figure 4.18: Class D amplifier with BPCM control.

	Designator	Value
Idle switching frequency	f_{Sw}	300 kHz
Output filter inductance	L	200 uH
DE Capacitance	C_{DE}	100 nF
Supply voltage	V_{CC}	$\pm$ 300 V
Closed-loop gain	A_V	43.5 dB

Table 4.2: Design parameters

index of 0.5). The carrier is given in figure 4.20 under idle operation. An idle switching frequency of 294 kHz is observed. This is acceptably close to the targeted 300 kHz.

Figure 4.21 shows the measured THD+N as function of the reference voltage for the frequencies of 100 Hz and 1 kHz. The THD+N is below 0.1% over a significant part of the operation range. Figure 4.22 presents the measured closed loop small-signal frequency response. The response is flat (within 5 dB) over the entire audio band, showing that active damping has been successfully implemented. Measurements are preformed using a voltage attenuation interface. The voltage attenuation interface is necessary in order to protect the input of the APX525 audio analyzer from the high operating voltages. Design and implementation of the voltage attenuation interface is addressed in [A1] and [101].

The measured efficiency is given in figure 4.23. The efficiency is defined in accordance

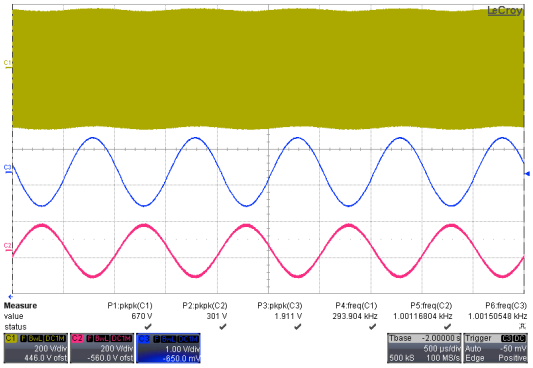


Figure 4.19: Waveforms of prototype amplifier. Top trace is the switching node voltage, the middle trace the reference voltage and the bottom the output voltage.

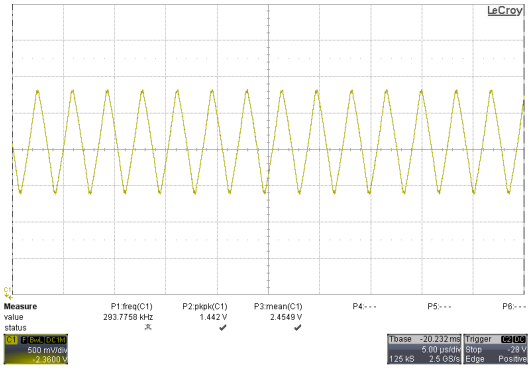


Figure 4.20: Carrier waveform operating at idle with switching frequency of 294 kHz.

with equation (2.5), and measured using the WT1600 power analyzer form Yokogawa. Note, that the efficiency at 100 Hz is below 42 %. Because the output voltage is kept fixed with respect to frequency, the reactive output power will drop inversely proportional with frequency. At 100 Hz the switching loss becomes comparable with the reactive output power. In the loss analysis of section 4.1.2 the ZVS range of the half-bridge power stage is not considered. The dead-time is assumed fixed and calculated as the optimum at M = 0. Because the inductor ripple current decreases with modulation index, the ZVS ability of the half-bridge power stage will decrease as well. As a consequence the switching loss starts to emerge for M different than zero. Increasing the dead-time will solve this problem, however at the expense of the THD+N. An efficiency above 90 % is achieved for the reference frequency of 3.5 kHz. Voltage mode control was selected in Chapter 2.

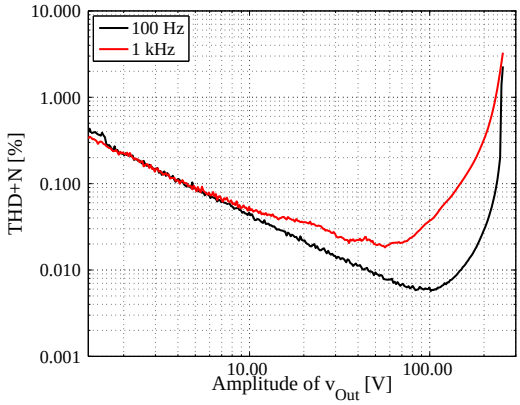


Figure 4.21: Measured THD+N of the prototype amplifier.

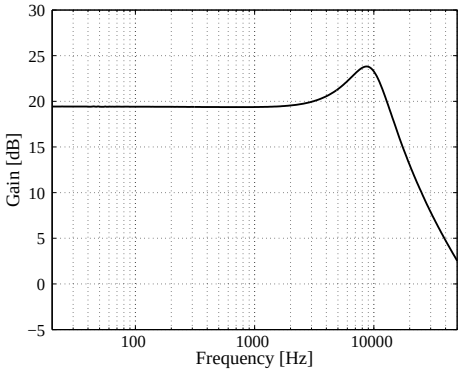


Figure 4.22: Measured closed-loop response of the prototype amplifier.

4.3 Fourth order output filter

The need for a fourth order output filter is divided into two:

- The DEAP transducer is not capacitive for frequencies above 10 kHz as shown

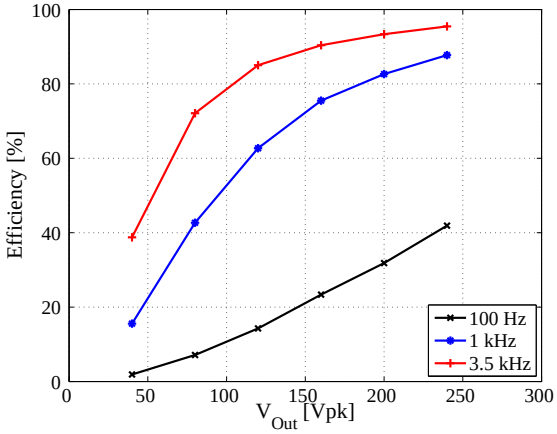


Figure 4.23: Measured efficiency of second order output filter prototype amplifier.

in figure 3.3. Accordingly the DEAP transducer is not a suitable choice for the output filter capacitance, when switching frequencies in the range of 100 kHz is targeted. It is proposed to use a film capacitor for the first LC-filter stage. The high frequency content will then bypass the DEAP transducer.

- The series resistance of the DEAP is an going research subject within the ATF project, and related to WP 2 of figure 1.3. Older versions of the DEAP transducer exhibited series resistance up to 50 Ω [76], while the present versions are specified within the region of 1–10 Ω. The connection between the DEAP transducer and the surrounding electronics is even more complicated than that of the film capacitor as the contact is performed on a surface exposed to significant mechanical stress.

Due to the high series resistance of the DEAP transducer, the magnitude of the ripple current becomes a concern. Conduction losses will dominate, if the ripple current becomes to high. This is both a problem in terms of efficiency, but also because of the reduced lifetime of the contact interface. In order to estimate the conduction loss in the series resistance of the DEAP transducer with second and fourth order output filtering, respectively, consider the Fourier series representing of a pulse-width modulation signal (D = 0.5) [63]

$$v_{PWM}(t) = \frac{4V_{CC}}{\pi} sin(2\pi ft) + \frac{4V_{CC}}{3\pi} sin(3 \cdot 2\pi ft) \tag{4.24}$$

$$\frac{4V_{CC}}{5\pi} sin(5 \cdot 2\pi ft) + \ldots \tag{4.25}$$

Using fundamental component analysis it can be assumed that

$$v_{PWM}(t) \approx \frac{4V_{CC}}{\pi} sin(2\pi ft) \tag{4.26}$$

The transfer function from input voltage to capacitor current for the second order output filter is

$$\frac{i_{DEAP}(s)}{v_{PWM}(s)} = \frac{C_{DEAP}s}{C_{DEAP}L_1 s^2 + \frac{L}{R}s + 1} \tag{4.27}$$

If a signal frequency is applied well above $\omega_0 = \frac{1}{\sqrt{L_1 C_{DEAP}}}$, equation (4.27) can be simplified to

$$\left| \frac{i_{DEAP}(j\omega)}{v_{PWM}(j\omega)} \right|_{\omega \gg \omega_0} \cong \frac{1}{L_1 \omega} \tag{4.28}$$

The current ripple is found by multiplying equation (4.26) with equation (4.31)

$$\Delta i_{DEAP} = \frac{2V_{CC}}{\pi^2 Lf} \tag{4.29}$$

For the fourth order output filter a similar approach can show that

$$\frac{i_{DEAP}(s)}{v_{PWM}(s)} = \frac{C_{DEAP}s}{s^4 L_1 L_2 C_1 C_{DEAP} + s^3 \frac{L_1 L_2 C_1}{R} + s^2(L_1 C_{DEAP} + L_1 C_1 + L_2 C_{DEAP}) + s\frac{L_1 + L_2}{R} + 1} \tag{4.30}$$

$$\left| \frac{i_{DEAP}(j\omega)}{v_{PWM}(j\omega)} \right|_{\omega \gg \omega_0} \cong \frac{1}{L_1 L_2 C_1 \omega^3} \tag{4.31}$$

$$\Delta i_{DEAP} = \frac{V_{CC}}{2L_1 L_2 C_2 \pi^4 f^3} \tag{4.32}$$

Consider a case study where $V_{CC} = 300$ V, $L_1 = 200\mu H$ and $f_{Sw} = 285$ kHz, the current ripple through the DEAP transducer becomes $\Delta i_{DEAP} = \frac{2 \cdot 300V}{200\mu H 2\pi 285kHz} = 1.59$ A peak for the second order output filter solution. Assuming $L_1 = L_2 = 200\mu H$ and

	Designator	Value
Idle switching frequency	f_{Sw}	285 kHz
Output filter inductance	L_1	200 uH
Output filter inductance	L_2	200 uH
Output filter capacitance	C_1	100 nF
DEAP Capacitance	C_{DEAP}	100 nF
Supply voltage	$\pm V_{CC}$	$\pm$ 300 V
Closed loop gain	A_V	75 $\frac{V}{V}$

Table 4.3: Design parameters

$C_1 = 100nF$, $\Delta i_{DEAP} = \frac{300V}{2 \cdot 200\mu H 200\mu H 100nF \pi^4 (285kHz)^3} = 16.6$ mA peak for the fourth order output filter solution. With a worst case series resistance of 10 Ω, the second order output filter solution will yield a loss of 8.43 W, while the loss of the fourth order output filter solution is 0.92 mW. For an amplifier producing a maximum output power of 125 Var, the fourth order output filter solution becomes the right choice in terms of efficiency.

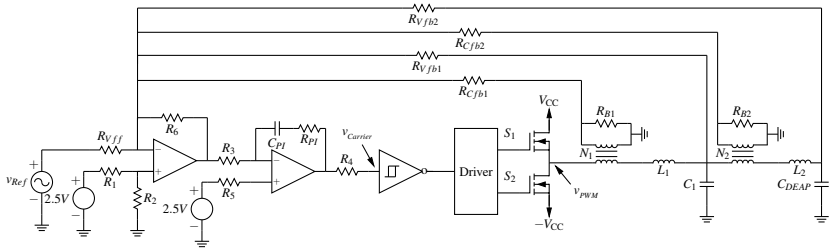
A $\pm$ 300 V half-bridge based prototype class D amplifier driving a 100 nF load in the midrange region of 0.1-3.5 kHz is used for experimental verification. Design parameters are presented in table 4.3. The self-oscillating hysteresis based BPCM control scheme utilised for the prototype amplifier is presented in figure 4.24(a), while figure 4.24(b) shows the small-signal model.

The measured efficiency can be seen in figure 4.25. At the reference frequency of 100 Hz, the efficiency stays below 40 %. An efficiency above 80 % is achieved for the reference frequencies of 1 and 3.5 kHz.

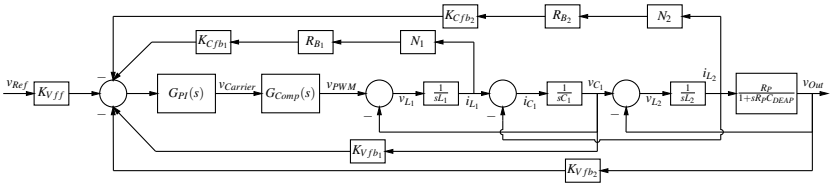
Figure 4.26 shows the measured THD+N as a function of the peak output voltage for the frequencies of 100 Hz and 1 kHz. THD+N is below 0.1% over a significant part of the operation range for the reference frequency of 100 Hz. Noise is the dominating factor especially for the 1 kHz measured THD+N.

4.4 Conclusion

The half-bridge power stage with second and fourth order output filters is utilised to implement audio amplifiers for DEAP transducers. Losses and pulse timing errors are discussed. A comparison between high voltage Si and SiC is conducted. It is shown that a peak efficiency above 80 % and THD+N below 0.1% can be achieved.



(a) Schematic with single-supply control circuitry.



(b) Small-signal model.

Figure 4.24: Prototype class D amplifier with fourth order output filter and control.

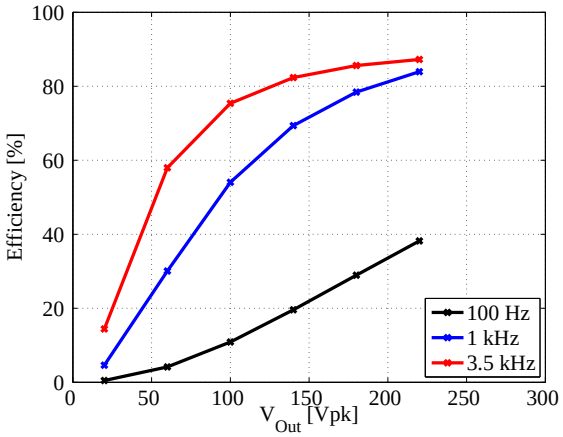


Figure 4.25: Measured efficiency of fourth order output filter prototype amplifier.

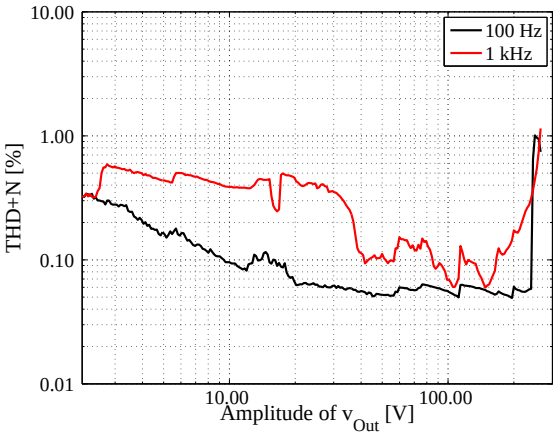


Figure 4.26: Measured THD+N of the prototype amplifier.

CHAPTER 5

N-Level modulators

The motivation for researching class D amplifiers based on multilevel inverters was divided into two:

- A single ended multilevel power stage using 600 V – 800 V MOSFETs, would allow for an increase in the achievable audio component, when compared with the half-bridge power stage. The increase being a multiple of the number of levels implemented. Also a single ended power stage would provide the option for direct drive using multiple levels or maintaining the separation of audio and biasing component approach of chapter 4. This was the subject of [A5].
- Development of a direct drive amplifier through phase shifting of two split supplied half-bridges. This was the subject of [A7].

5.1 Split supplied phase shifted half-bridges

Class D audio amplifiers driving the resistive and inductive load of the electrodynamic transducer are implemented using the half- and full-bridge power stages as shown in chapter 2. These power stages do not provide the DC-biasing voltage required by DEAP transducer. The half-bridge power stage can be modified to allow for DC-operation by using a single supply implementation as shown in figure 5.1. The configuration achieves a sinusoidal waveform with a peak amplitude of $\frac{V_{CC}}{2}$ at the corresponding DC-biasing voltage of $\frac{V_{CC}}{2}$. If a higher biasing voltage is targeted, it will be at the cost of reduced peak amplitude.

In order not to loose peak amplitude with DC-biasing the split supplied, phase shifted half-bridges class D power stage as shown in figure 5.2 is proposed. This configuration allows for operation at a DC-biasing voltage of V_{CC}, while the peak amplitude is V_{CC}. An inconvenient consequence of the split supplied, phase shifted half-bridges class D power stage is the cost of two extra MOSFETs, an output filter and a voltage source, when comparing with the half-bridge solution.

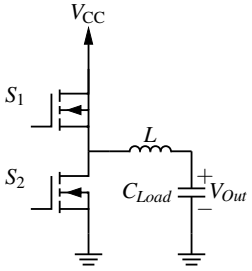


Figure 5.1: Half-brigde class D power stage.

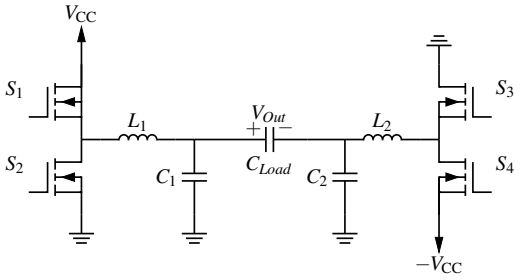


Figure 5.2: Split supplied, phase shifted half-bridges class D power stage.

The split supplied, phase shifted half-bridges class D power stage is constructed from two single supplied half-bridges. Each half-bridge power stage has its own control scheme. The hysteresis based self-oscillating BPCM control scheme, as presented in chapter 4, is used. A conceptual diagram of the complete differential coupled class D power stage is shown in figure 5.3. The half-bridges are operated at a 180^o phase shift, and a synchronisation circuit ensures, that no unwanted frequencies folds into the audio band.

5.1.1 Synchronisation of multiple carriers

Synchronisation of multiple carriers is a known issue in three-level modulated full-bridge class D amplifiers. Self-oscillating systems have an inherent tendency of locking

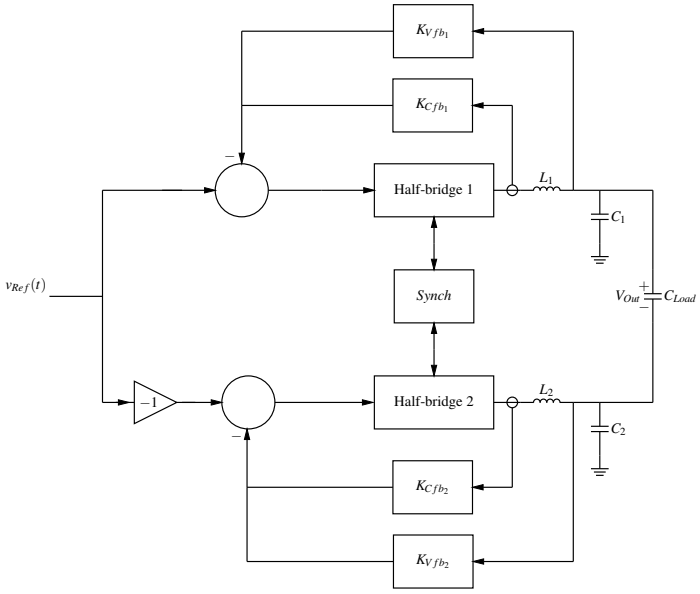


Figure 5.3: A conceptual diagram of the complete split supplied, phase shifted half-bridges class D power stage.

to external frequencies. As proposed in [26] a simple high impedance path between two oscillators, will cause these to synchronise. Figure 5.4 shows, how two carriers can be synchronised using coupled hysteresis windows.

The key design parameters of the prototype amplifier are collected in table 5.1. Figure 5.5 shows the differential switching node and output voltages, when operating at a reference frequency of 100 Hz and output voltage of 250 V_{pkpk}. The DC-biasing voltage is 400 V corresponding to a duty cycle of 0.5. An idle switching frequency of 84 kHz is observed.

	Designator	Value
Idle switching frequency	f_{Sw}	84 kHz
Output filter inductance	L_1 and L_2	300 uH
Load capacitance	C_{Load}	100 nF
Supply voltage	$\pm V_{CC}$	$\pm$ 400 V
Filter capacitance	C_1 and C_2	100 nF
Closed loop voltage gain		48 dB

Table 5.1: Design parameters

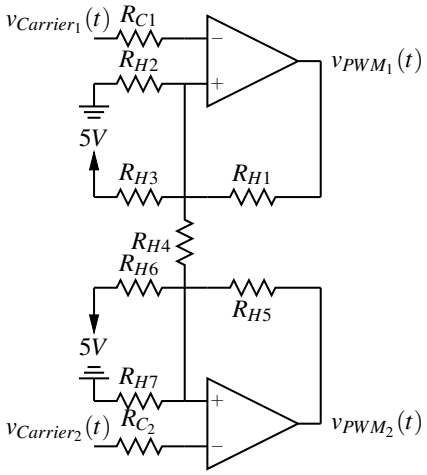


Figure 5.4: Synchronisation of multiple carriers.

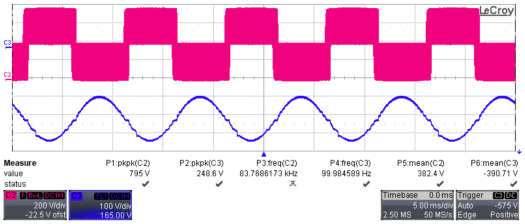


Figure 5.5: Differential switching node and output voltages, when operating with a reference frequency of 100 Hz and output voltage of 250 V_{pkpk}.

Figure 5.6 gives the measured THD+N as function of the reference voltage for the frequencies of 100 Hz and 1 kHz. THD+N is below 2% over a significant part of the operation range for the reference frequency of 100 Hz. All measurements are performed using a 4 kHz low-pass filter. This is valid, because the amplifier is targeting the midrange region of the audio band (100 Hz – 3.5 kHz). A class D audio amplifier with split supplied, phase shifted half-bridges is proposed. The amplifier addresses the issue of driving a capacitive transducer under biasing.

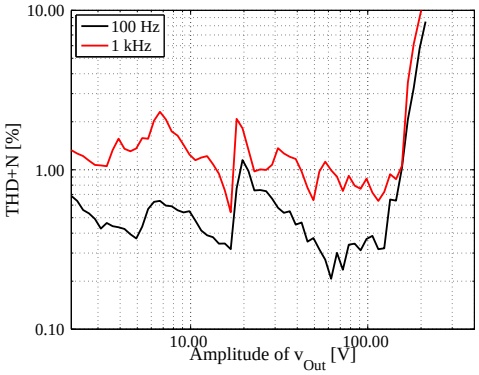


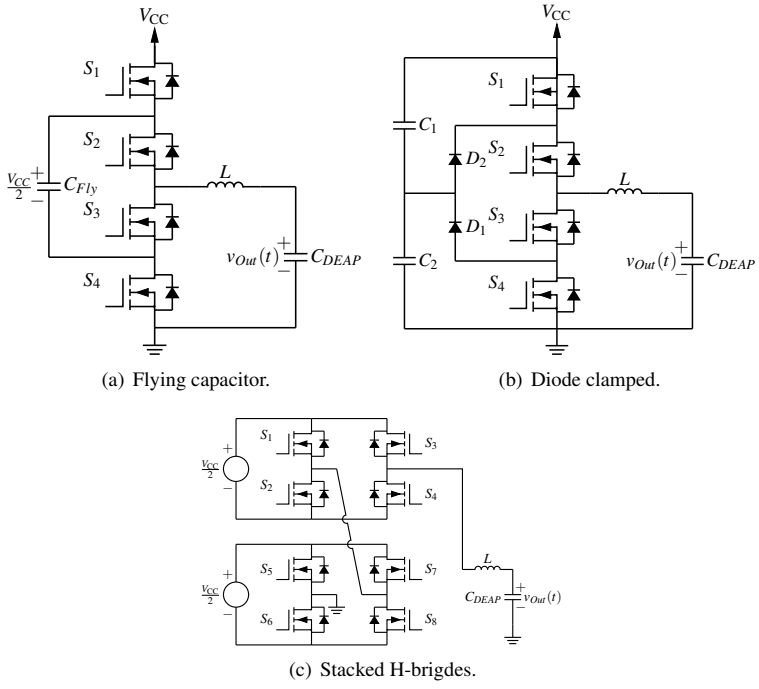
Figure 5.6: THD+N (100 Hz and 1 kHz).

5.2 3-Level flying capacitor

The three fundamental configurations of the multilevel inverters are the flying capacitor, diode clamped and stacked H-brigdes [102, 103, 104]. Figure 5.7 illustrates the three level version of each of these three configurations. Each configuration can be extended to higher levels if necessary. The flying capacitor configuration is advantageous, because of its low number of semiconductors, and the fact that it does not require isolated sources. Diodes are further more not a good choice for audio applications due to their nonlinear characteristic. Maintaining the charge balance of C_{Fly} is on the other hand a concern for the flying capacitor configuration. This is one of the reasons, why flying capacitor inverters have not been used for class D amplifiers [25]. The zero ripple current at idle is however an interesting property, which some authors prefer in the pursuit of lowering the idle losses [105].

5.2.1 Balancing the flying capacitor

When selecting a flying capacitor power stage, balancing the charge of C_{Fly} becomes a key concern. A number of publications have dealt with the issue of balancing the charge of the flying capacitor and lowering the voltage ripple with suitable modulations schemes [106, 107]. These publications assume the inductive and resistive load found in motor drive applications. An important concept is the flying capacitor self- or natural-balancing [108]. It is suggested in [108], that a capacitive load will not necessary ensure natural-balancing. Consequently it is proposed to implement force balancing. A very simple way of implementing active or forced balancing is intro-



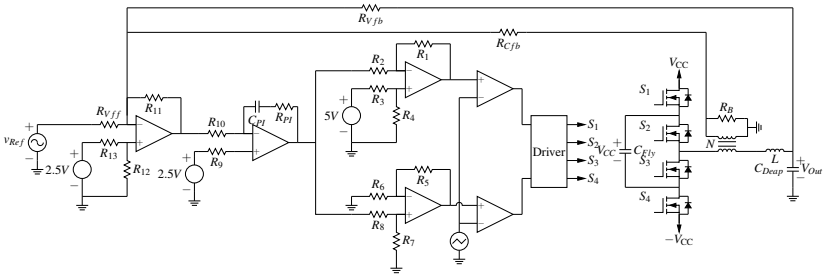
(a) Flying capacitor.

(b) Diode clamped.

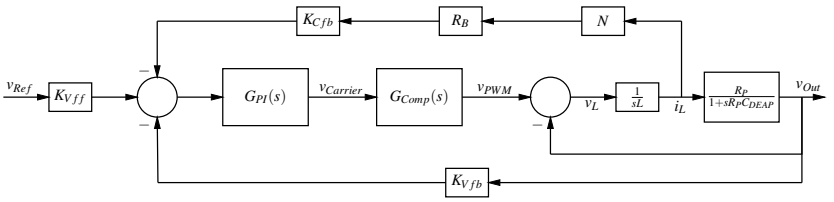
(c) Stacked H-brigdes.

Figure 5.7: Fundamental multilevel inverter configurations.

duced in [109] by control of the inductor current. This approach is particular suitable for the application of a DEAP transducer, as the current loop effectively balance the charge between C_{Fly} and C_{DEAP}. Figure 5.8(a) shows a schematic of the power stage with control. The inductor current is sensed through a current sense transformer. Low frequency loop gain is achieved by the addition of a voltage loop. A PI-controller is used under fixed frequency operation. Phase shifted error signals are utilised for generating the three level PWM signal. A small-signal model of the amplifier is given in figure 5.8(b). $G_{Comp}(s)$ is the combined small-signal transfer function of comparators and power stage.



(a) Schematic with single-supply control circuitry.



(b) Small-signal model.

Figure 5.8: Flying capacitor class D amplifier with control.

Table 5.2 shows the key design parameters of the prototype amplifier. Time domain waveforms are given in figure 5.9 for the reference frequency of 1 kHz and a modulation index of 0.67.

Figure 5.10 shows the measured THD+N as a function of the peak output voltage for the frequencies of 100 Hz and 1 kHz. THD+N is below 2% over a significant part of the operation range. Noise is the dominating factor at low amplitudes. As the signal-to-noise ratio improves, the THD+N drops linearly until it reaches an amplitude of 10 V. Above 10 V harmonic distortion dominates before clipping.

The concept of multilevel inverters as power stages in class D audio amplifiers is introduced. It is proposed to drive capacitive transducers from a three-level modulated

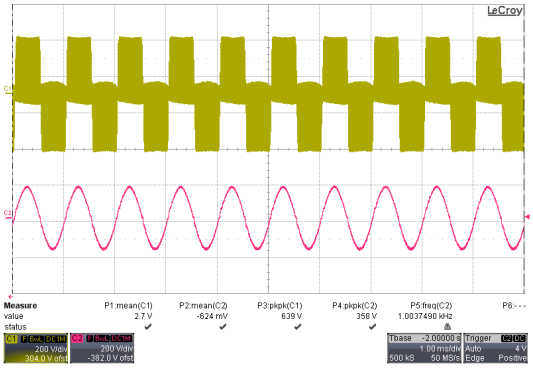


Figure 5.9: Time domain waveforms with a reference frequency of 1 kHz and modulation index of 0.66. The switching node voltage is the top trace, while the output voltage is the bottom trace.

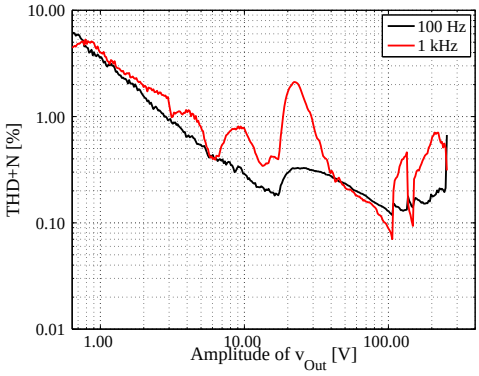


Figure 5.10: Measured THD+N of the prototype amplifier.

flying capacitor class D amplifier. Experimental verification is conducted on a $\pm$ 300 V prototype amplifier driving a 100 nF load in the midrange region of 0.1-3.5 kHz. THD+N below 2 % is reported over a significant part of the operation range. The main challenge is achieving ZVS. At idle no ripple current will run through the output filter inductor, and ZVS is not be possible. This causes significant switching losses at idle. In order to benefit from the full potential of the multilevel flying capacitor inverter, research into ZVS should be conducted.

	Designator	Value
Switching frequency	f_{Sw}	167 kHz
Output filter inductance	L	200 uH
DEAP Capacitance	C_{DEAP}	100 nF
Flying Capacitance	C_{Fly}	100 nF
Supply voltage	$\pm V_S$	$\pm 300V$
Closed loop gain	A_V	150 $\frac{V}{V}$

Table 5.2: Design parameters.

5.3 Conclusion

The subject of N-Level modulators is investigated though the implementation of the three-level modulated phase shifted half-bridges and flying capacitor multilevel inverter. It is shown that both amplifiers suffer from a high noise floor, motivating further research into coupling of self-oscillating modulators, and the ZVS abilities of the flying capacitor multilevel inverter. N-level modulators is a key enable for the DEAP technology as the reduced semiconductor stress allows the designer of the amplifier to select from a larger variety of MOSFETs. This is beneficial not only in terms of performance, but also cost.

CHAPTER 6

Conclusion and future work

6.1 Conclusion

The work presented in this thesis and the assisted publications are related to research within class D audio amplifiers for high voltage capacitive transducers. A number of class D amplifiers with active damping for DEAP transducers is presented. Showing, that the technology of switched mode based class D audio amplifiers can be utilised for the application of driving high voltage, capacitive transducers. The major contributions of this thesis in the path of obtaining the goal of high efficient capacitive based loudspeaker systems are listed below.

- Characterisation of the DEAP transducer through impedance measurements. The purpose was to gain an understanding of the impedance, which the power amplifier is to drive. It is concluded that the present version of the DEAP transducer can be modelled as a static capacitor within the audio band. For the biasing voltages considered, a maximum change in the static capacitance of 10 % is reported.
- Full-state variable feedback second order hysteresis based self-oscillation amplifier with active damping driving capacitive transducers for audio applications.
- Full-state variable feedback fourth order hysteresis based self-oscillation amplifier with active damping driving capacitive transducers for audio applications.
- Investigation of SiC and Si MOSFETs for the application of high voltage, capacitive loaded class D amplifiers.
- Three-level flying capacitor multilevel inverter with active damping and charge balancing driving capacitive transducers for audio applications.

- Direct drive class D audio amplifier for capacitive transducers.

6.2 Future work

This section presents a selection of topics related to the future work on the subject of DEAP based audio systems. Emphasis is placed upon research activities, critical to the pursuit of commercialisation of the DEAP technology in high performance drives.

- Investigation of the full system efficiency including the two subsystems of the amplifier and loudspeaker. Measuring the real power assumed by the transducer is a particular challenge.
- On the side of the DEAP material significant improvement is needed in order to ensure the success of the DEAP technology in audio applications. Lowering the capacitance, while increasing the displacement is critical. Also the mechanical resonances of the DEAP film must be dealt with, either by introducing damping or through a deeper understanding of their origin, allowing the designer to place them outside the considered part of the audio band. The frequency response and series resistance of the DEAP transducer is a concern as well. If the DEAP transducer are to be used as the sole output filter capacitor in an amplifier with second order output filter, the DEAP transducer should be capacitive to at least 1 MHz. Thermal modelling of the heat dissipation in the series resistance of the DEAP transducer is a subject. This is needed, in order to establish the maximum power that can be supplied to the DEAP transducer.
- Non-proportional gain power stages for high performance capacitive transducers. The flyback converter is a particular interesting candidate for a direct drive solution. Sigma-delta modulation allowing the flyback transformer to reset between each PWM pulse is a subject of interest.
- Investigation of the difference between voltage, current and charge mode control from both an electrical, mechanical and acoustical perspective.
- Implementation of a DC-linked based amplifier operating from the mains. The flyback converter is a particular interesting candidate for implementing the DC-link. Dual windings on the secondary side of the flyback converter will allow for both the amplifier supply and biasing voltage to be generated in a isolated fashion.
- Investigation of isolation strategies. The current implemented prototypes uses current sense transformers in order to extract high frequency information from the power stage in an isolated fashion. The low frequency content is achieve

through a voltage divider. Linearity of optocouplers should be investigated in order to ensure isolation of the reference signal.

- Current limitation strategy in voltage mode control amplifiers for capacitive loads. Voltage mode control is preferred in the thesis. The high peak current, associated with a step response applied to the DEAP transducer, is a concern. Semiconductor current limitations, output filter inductor saturation and power supply pumping are all issues related to the peak DEAP current. Research into a soft current limiter circuit should be conducted. Also, the consequences related to the acoustic perception during a current limiting event, could be investigated.

- The ripple current of the three-level modulated flying capacitor inverter at idle is zero. Consequently, soft switching can not be achieved by just ensuring sufficient deadtime, as was the case with the half-bridge power stage. Additional research is to be conducted on the soft switching abilities of multilevel flying capacitor inverters. Soft switching is key in terms of efficiency, but also with respect to dv/dt induced turn on of the MOSFETs.

- For the purpose of implementing a full amplifier system operating from the mains, research, into a low impedance, high voltage biasing source, should be conducted.

- Investigate the usage of JFETs and IGBTs for the amplifier power stage. Research, documenting the linearity and efficiency of the two technologies, should be conducted.

- Upstart circuitry for multilevel level flying capacitor inverters, ensuring that the semiconductor voltage stress is not violated during start up.

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Appendix

A: List of publications

Overview of publications accomplished during this PhD study. The publications are located in appendix A.

- A1: "Driving electrostatic transducers", **Dennis Nielsen**, Arnold Knott and Michael A.E. Andersen, AES 134, 2013, Rome, Italy.
- A2: "Charachterization of Dielectric Electroactive Polymer Transducers", **Dennis Nielsen**, Martin Bo Møller, Rahimullah, Benny Lassen, Arnold Knott and Michael A.E. Andersen, SPIE Smart Structures and Materials, 2014, San Diego, US.
- A3: "Hysteretic self-oscillating bandpass current mode control for class D audio amplifiers driving capacitive transducers", **Dennis Nielsen**, Arnold Knott and Michael A. E. Andersen, ECCE Asia Downunder (ECCE Asia), 2013.
- A4: "A high-voltage class D audio amplifier for dielectric elastomer transducers", **Dennis Nielsen**, Arnold Knott and Michael A. E. Andersen, Applied Power Electronics Conference and Exposition (APEC), 2014.
- A5: "Multilevel inverter based class D audio amplifier for capacitive transducers", **Dennis Nielsen**, Arnold Knott and Michael A.E. Andersen, 16th Conference on Power Electronics and Applications, EPE14-ECCE Europe, Lappeenranta, Finland.
- A6: "Class D audio amplifier with 4th order output filter and self-oscillating full-state hysteresis based feedback driving capacitive transducers", **Dennis Nielsen**, Arnold Knott and Michael A.E. Andersen, 16th Conference on Power Electronics and Applications, EPE14-ECCE Europe, Lappeenranta, Finland.
- A7: "A Direct Driver for Electrostatic Transducers", **Dennis Nielsen**, Arnold Knott and Michael A. E. Andersen, 137 AES Convention, LA, USA.
- A8: "Comparative Study of Si and SiC MOSFETs for High Voltage Class D Audio Amplifiers", **Dennis Nielsen**, Arnold Knott and Michael A. E. Andersen, 137 AES Convention, LA, USA.
- A9: "Pre-distortion of audio circuits", Thomas Haggen Birch, **Dennis Nielsen** and Arnold Knott, 137 AES Convention, LA, USA.

[A1]

Dennis Nielsen, Arnold Knott and Michael A.E. Andersen, "Driving electrostatic transducers", AES 134, 2013, Rome, Italy.

Audio Engineering Society

Convention Paper

Presented at the 134th Convention
2013 May 4–7 Rome, Italy

Driving electrostatic transducers

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ABSTRACT

Electrostatic transducers represent a very interesting alternative to the traditional inefficient electrodynamic transducers. In order to establish the full potential of these transducers, power amplifiers which fulfill the strict requirements imposed by such loads (high impedance, frequency depended, nonlinear and high bias voltage for linearization) must be developed. This paper analyzes power stages and bias configurations suitable for driving an electrostatic transducer. Measurement results of a $\pm$ 300 V prototype amplifier are shown. Measuring THD across a high impedance source is discussed, and a high voltage attenuation interface for an audio analyzer is presented. THD below 0.1% is reported.

1. INTRODUCTION

Switch-mode audio power amplifiers are commonly used in sound reproduction driving electrodynamic transducers. While these audio systems are dominating the market of sound reproduction, they still suffer from the poor efficiency imposed by the electrodynamic transducer. As a consequence the audio community is constantly searching for new high efficient audio transducers. An alternative to the electrodynamic transducer is the electrostatic transducer. Electrostatic transducers are most known from their usage in electrostatic loudspeakers, however Dielectric Electro Active Polymers (DEAP) can also be used to form an electrostatic transducer. A DEAP transducer is shown in figure 1. Electrostatic transducers present a high impedance and frequency depended nonlinear load to the amplifier. Commercial electrostatic loudspeakers are driven from tube, linear or audio-transformer based amplifier solutions. Consequently these systems suffer from being bulky, fragile and inefficient. In order to establish the full potential of the electrostatic transducer, a new generation of audio amplifiers must be developed. These amplifiers should have a high power density, low power loss and be robust. Accordingly it is proposed to use a switch-mode audio amplifier or class D amplifier for driving the electrostatic transducer. Switch-mode audio amplifiers are known for their low power consumption, high power density and excellent audio figures (for instance low Total Harmonic Distortion or THD). However high voltage switch-mode audio power amplifiers driving a capacitive load without the use of audio or high frequency linked transformers, is an area of research with little to no publications. This paper analyzes power stages and bias configurations suitable for driving electrostatic transducers.

Figure 1: *DEAP transducer.*

1.1. Electrostatics

Like a traditional electrostatic loudspeaker, the electrostatic pressure of the DEAP transducer exhibits squared dependency on the applied voltage [1, 2]

$$\sigma(t) = \varepsilon_0 \varepsilon_r \left(\frac{v_c(t)}{d} \right)^2 \quad (1)$$

with ε_0 being the permittivity of vacuum, ε_r, the relative permittivity of the Dielectric Electro (DE) material and d the distance between the electrodes.

Assume a voltage consisting of a DC and an audio component:

$$v_c(t) = v_{Bias} + v_{Audio} cos(2\pi f t) \quad (2)$$

It can be shown that:

$$v_c^2(t) = v_{Bias}^2 + v_{Audio}^2 cos^2(2\pi f t) \quad (3)$$
$$+2 v_{Bias} v_{Audio} cos(2\pi f t) \quad (4)$$
$$v_c^2(t) = v_{Bias}^2 + v_{Audio}^2 \left(\frac{1 + cos(4\pi f t)}{2} \right) \quad (5)$$
$$+2 v_{Bias} v_{Audio} cos(2\pi f t) \quad (6)$$

From equation (6) the THD can be derived:

$$THD = \frac{\frac{v_{Audio}^2}{2}}{2 v_{Bias} v_{Audio}} = \frac{v_{Audio}}{4 v_{Bias}} \quad (7)$$

Consequently $v_{Bias} > 25 v_{Audio}$ in order to reach THD below 1%. Proper biasing is thus of key importance, when driving a electrostatic transducer. Not only does biasing improve the linearity of the transducer, the electrostatic pressure also rises with the square of the biasing voltage. Typically the applied biasing voltage will be limited by the break-down voltage of the dielectric material. Figure 2 shows the electrostatic pressure as a function of the biasing voltage (equation (1)), while figure 3 gives the THD as a function of the biasing voltage with a selection of audio amplitudes imposed (equation (7)). The figures are constructed using $\varepsilon_r = 3.1$, $\varepsilon_0 = 8.8542 \frac{C}{Vm}$ and $d = 80\mu m$, which are the parameters of the DEAP transducer in figure 1.

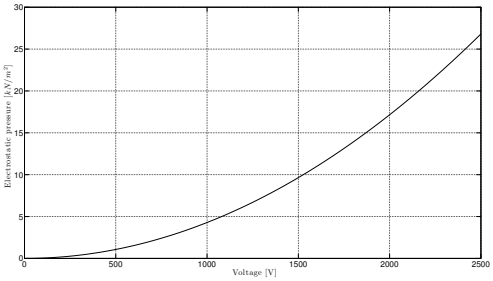


Figure 2: *Electrostatic pressure of DEAP vs. bias voltage.*

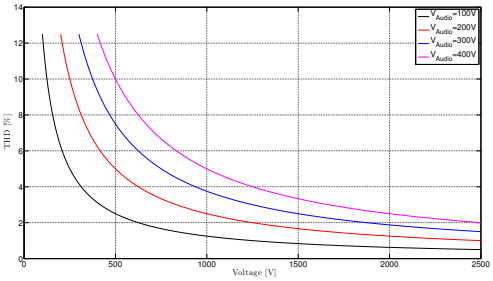


Figure 3: *THD of DEAP vs. bias voltage.*

2. ANALYSIS

The application of DEAP transducers for audio reproduction has been considered in [3, 4], though without addressing the audio amplifier design. Models of DEAP transducers can be found in [5, 1], suggesting that the

transducer is to be considered as a capacitor with a parallel and a series resistance. For the analysis of this paper a first order approach will be used, modeling the DEAP transducer as a pure capacitor. Influence of series and parallel resistance will be the subject of a future publication.

2.1. Power stage

When driving an electrostatic transducer one must first establish, which power stage are most suitable for the task at hand. Several publications exists analyzing class A, B, AB and D power stages driving a traditional electrodynamic loudspeaker setup [6, 7]. First order approximation are utilized, assuming that the loudspeaker setup represent a restive load. It is concluded, that class D power stages provide significant advantage in terms of efficiency, stressing their position in the market of audio reproduction [6, 7]. This section will briefly preform the same analysis assuming a capacitive load.

2.1.1. Linear amplifiers

Some authors have already taken on the task of analyzing and comparing capacitive loaded amplifiers [8, 9, 10]. However the findings of these analysis are scattered to say the least. One author suggest, that a efficient class D power stage easily can be obtained [11], while another prefer the class B [8].

Before proceeding with the analysis it is appropriate to give a formal definition of the term efficiency. When driving an ideal electrostatic transducer, no real power will be delivered to the load, and it is thus appropriated to define the efficiency as

$$\eta = \frac{P_{Out}}{P_{Out}+P_{In}} \tag{8}$$

where $P_{Out} = \frac{V_{rms}^2}{\left(\frac{1}{\omega C_{Deap}}\right)}$, the reactive power delivered to the load, and P_{In} corresponds to the real power consumed by the amplifier.

Let us consider the ideal Class B amplifier as representative of the linear amplifiers. A Class AB amplifier would probably be preferable in all practical applications, however the inclusion of quiescent losses is beyond the scope of this simple 1. order analysis. Assuming $v_{Out}(t) = \hat{V} sin(\omega t)$ the input power of the Class B amplifier shown in figure 4 can be calculated as

$$P_{In} = \frac{\omega}{2\pi}\int_0^{\frac{\pi}{\omega}} V_{CC}\frac{\hat{V} sin(\omega t)}{\left(\frac{1}{\omega C_{Deap}}\right)}\mathrm{d}t \tag{9}$$

$$= \frac{V_{CC}\hat{V}C_{Deap}\omega}{\pi} \tag{10}$$

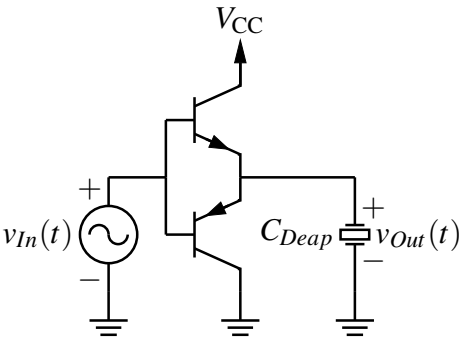


Figure 4: *Class B amplifier with capacitive load.*

The efficiency then becomes

$$\eta = \frac{\frac{\hat{V}^2\omega C_{Deap}}{2}}{\frac{\hat{V}^2\omega C_{Deap}}{2}+\frac{V_{CC}\hat{V}C_{Deap}\omega}{\pi}} \tag{11}$$

$$= \frac{\frac{\hat{V}}{2}}{\frac{\hat{V}}{2}+\frac{V_{CC}}{\pi}} \tag{12}$$

For $\frac{V_{CC}}{2} = \hat{V}$ the efficiency reaches its maximum

$$\eta_{Max} = \frac{\pi}{\pi+4} \tag{13}$$

The theoretical maximum efficiency of $\frac{\pi}{\pi+4} = 44.0\%$ for the class B amplifier, justifies the pursuit of a switch-mode amplifier as the DEAP driver. Notice that a class B amplifier driving a capacitive load will have a significant smaller efficiency than the 78% maximum efficiency of one driving a resistive load [6]. A switch-mode amplifier will have a theoretical efficiency of 100 % using a first order approximation. Detailed analysis of switching and conduction losses in a capacitive loaded switch-mode amplifier is beyond the scope of this paper.

2.2. Biasing

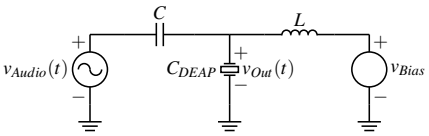
Fundamentally two different approaches can be adopted, when driving a load in the need of biasing. One is to build a direct-drive amplifier, which can provide both the bias and the audio component. Another is to separate the bias and audio into two independent sources. The later configuration will be preferable, if a transformerless approach is adapted (no use of audio or high frequency linked transformers). Direct-drive will typically

require semiconductors with voltage rating far beyond, what is commercial available. The DEAP transducer of figure 1 can be operated at a maximum voltage of 2.5kV, and while some commercial Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) and Insulated-Gate Bipolar Transistor (IGBTs) can handle such voltages, they are not suitable for the switching frequencies required by switch-mode audio amplifiers. An interesting alternative to MOSFETs and IGBTs are their silicon carbide (SiC) counterparts. However these semiconductors are still at an early stage of development with limited (and expensive) quantities and drivers commercial available.

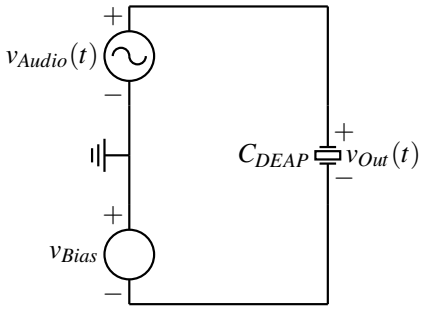
Breaking up the audio and bias component into two separate components (sources), allows for the use of MOSFETs with voltage ratings in the range of 600–800 V for the audio source. A number of ways for implementing such configurations are depicted in figure 5. Figure 5(a) and 5(b) illustrate drive configurations for a two terminal push DEAP transducer like the one shown in figure 1, while figure 5(c) and 5(d) represents push-pull configurations. Notice how figure 5(c) corresponds to the "traditional" way of driving an electrostatic loudspeaker [2] typically implemented using an audio-transformer. The main difference between 5(a) and the rest is, that a high voltage DC blocking capacitor together with a coupling inductor is needed. Especially the DC blocking capacitor is troublesome, as it must be rated for the full bias voltage, and must be significant larger than the DEAP capacitance in order to provide a low impedance path for audio component. In the configurations of figure 5(b), 5(c) and 5(d) the output impedance of the biasing source is very important, as the audio should be presented to a low impedance path, which does not add THD. The complex interaction of series connected sources and their control schemes will not be considered in this paper. A switch-mode class D audio amplifier capable of delivering the audio component in configurations like the ones seen in figure 5(b) and 5(d) will be presented in the following section.

3. PROTOTYPING

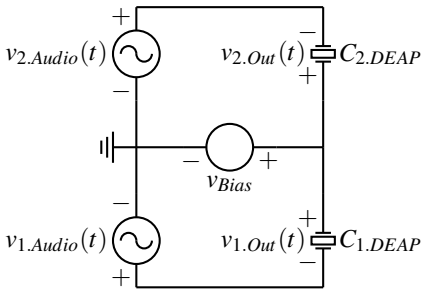
The prototype amplifier shown in figure 6 is based on a Si8235 digital isolated gate driver and SPA08N80C3 MOSFET's. A single supply self-oscillating control scheme has been selected similar to the one of [12]. A two loop configuration known as BPCM (Band-Pass Current Mode) ensures current control of the switching frequency component, while a slow outer voltage loop allows for loop gain within the audio bandwidth. This prototype



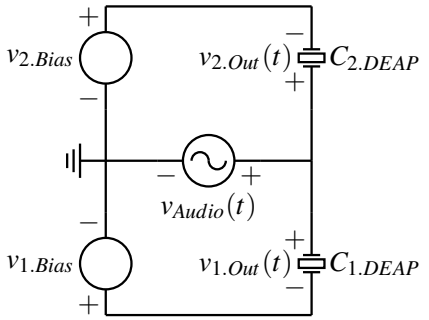
(a) DC-blocking



(b) Single stage or stacking configuration.



(c) Push-pull with dual audio stage.



(d) Push-pull with single audio stage.

Figure 5: *Biasing configurations.*

Table 1: *Key parameters of the prototype*

	Designator	Value
Idle switching frequency	f_{Sw}	167 kHz
Output filter inductance	L	125 uH
DEAP Capacitance	C	100 nF
Supply voltage	$\pm V_{CC}$	$\pm 300V$
Output filter resonance filter	f_r	35 kHz
Closed loop gain	A_V	150 $\frac{V}{V}$

utilizes a half-bridge power stage for simplicity. The key parameters of the prototype are gathered in table 1. All measurements are preformed using a polypropylene capacitor as dummy load. The output filter capacitance is considered as the load capacitance.

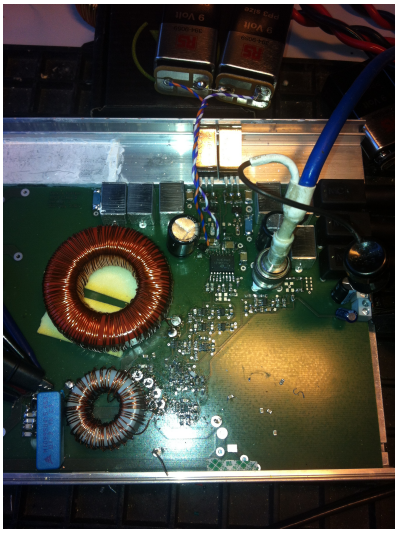


Figure 6: *Prototype amplifier.*

It is beyond the scope of this paper to describe the control scheme implemented in the prototype. However an detailed analysis of the subject can be found in [12].

4. MEASUREMENT RESULTS

Time domain waveforms are shown in figure 7 for the switching node, reference and output voltages. The reference voltage of 1.5 V corresponds to a modulation index of 0.75.

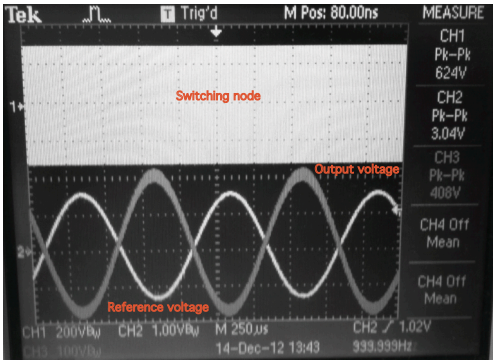


Figure 7: *Time domain waveforms with a reference frequency of 1 kHz and modulation index of 0.75.*

4.1. THD from a high impedance source

THD measurements are complicated by the high voltage operation constraints. No commercial available audio analyzers can handle voltages in the range of $\pm 300V$ or above. Accordingly a step-down interface must be constructed. The linearity of this interface is of the key-interest. A passive interface is suggested by [13], consisting of a simple voltage divider and a capacitor compensating for the input capacitance of the audio analyzer. Figure 8 illustrates the measuring setup. If $R_1C_1 = R_2C_2$, a flat response is guaranteed. It is recommended to use ceramic capacitors of the type C0G or NP0 in order to maintain linearity [14].

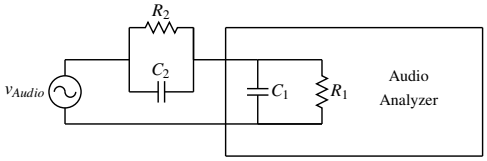


Figure 8: *THD measuring setup.*

Figure 9 shows the frequency response of the step-down interface. The interface gives 27 dB of attenuation. Figure 9 also shows the case of $C_2 = 0$, causing the response to drop off within the audio bandwidth, resulting in an

invalid measurement. C_2 is tuned to ensure a flat response within $\pm 0.2dB$ over the entire audio bandwidth.

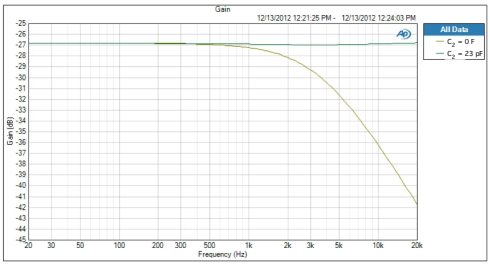


Figure 9: *Frequency response of the step-down interface.*

4.2. Prototype THD

THD measurements are shown in figure 10 for the reference frequencies of 100 Hz, 1 kHz and 6.67 kHz. An APX525 audio analyzer and the step-down interface of the above section were used to collect the data. THD is plotted as a function of the reference voltage with the closed loop gain of the amplifier being 43.5 dB. The THD goes below 0.1% over a significant part of the operation range.

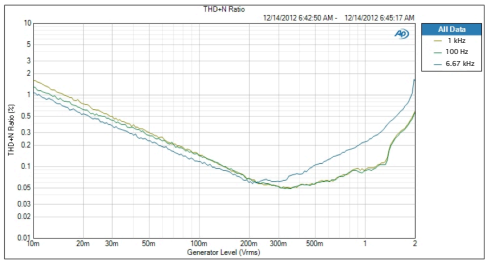


Figure 10: *THD of the prototype for the reference frequencies of 100 Hz, 1 kHz and 6.67 kHz.*

5. CONCLUSION

A half-bridge class D prototype amplifier supplied from $\pm$ 300 V has been demonstrated. The amplifier is suitable for providing the audio component in a configuration, where biasing and audio signals are achieved though two independent sources. Accordingly an electrostatic transducer can be driving without the need of a step-up audio or high frequency linked transformer. Measuring THD across a high impedance source was discussed. A high voltage attenuation interface has been built, allowing THD to be measured with an audio analyzer. THD below 0.1% is shown.

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Characterization of Dielectric Electroactive Polymer Transducers

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ABSTRACT

Throughout this paper, a small-signal model of the Dielectric Electro Active Polymer (DEAP) transducer is analyzed. The DEAP transducer have been proposed as an alternative to the electrodynamic transducer in sound reproduction systems. In order to understand how the DEAP transducer works, and provide guidelines for design optimization, accurate characterization of the transducer must be established. A small signal model of the DEAP transducer is derived and its validity is investigated using impedance measurements. Impedance measurements are shown for a push-pull DEAP based loudspeaker, and the dependency of the biasing voltage is explained. A measuring setup is proposed, which allows the impedance to be measured, while the DEAP transducer is connected to its biasing source.

Keywords: Dielectric electroactive polymers, lumped equivalent model, loudspeaker

1. INTRODUCTION

Electrodynamic transducers have dominated the market of sound reproduction for a century. The electrostatic transducer is proposed as a very interesting alternative to these inefficient and bulky transducers. Electrostatic transducers are most known from their usage in electrostatic loudspeakers, however Dielectric Electro Active Polymers (DEAP) can also be used to form an electrostatic transducer [1, 2, 3, 4, 5, 6, 7]. DEAP transducers are constructed by printing compliant electrodes on both sides of a silicone membrane. In order to design not only the loudspeaker itself, but also the amplifier driving the DEAP transducer, the small-signal model of the DEAP transducer must be known. Such a model will allow for the frequency response, efficiency and input impedance of the DEAP transducer to be analyzed.

In this paper, the small-signal model of the DEAP transducer is analyzed through its input impedance. Electrodynamic transducers and their input impedance are well documented [8]. Also models of the electrostatic loudspeaker can be found in the literature [9], however with little experimental data backing the theory. The theory of the electrostatic loudspeaker shows, that the loudspeaker can not be considered as a pure capacitance at high bias voltage [9]. As the voltage is increased the mechanical resonances of the loudspeaker appear in the impedance. This information is key for the design of the amplifier driving the electrostatic loudspeaker. While the electrostatic loudspeaker and the DEAP transducer based loudspeaker both rely on the forces of electrostatics, the change in capacitance is not comparable. Accordingly a new model must be derived for DEAP transducer based loudspeakers. The validity of the model is investigated using measurements of the input impedance. A measuring-setup is proposed, allowing for the impedance of the DEAP transducer to be measured under the influence of a biasing voltage. Measurements are presented under different biasing conditions.

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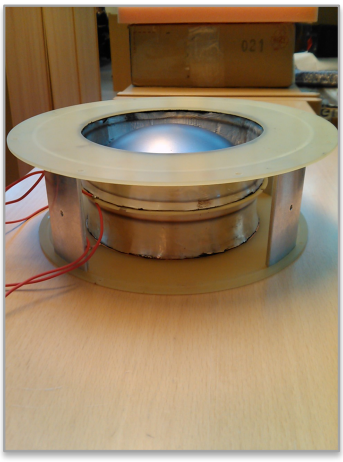
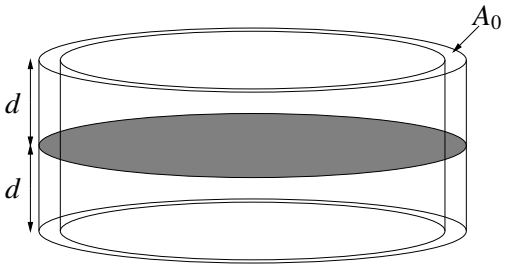


(a) Picture of the prototype.



(b) Sketch with geometric parameters specified.

Figure 1: *Push-pull DEAP transducer based loudspeaker.*

2. THEORY

The transducer investigated throughout this paper is based on a silicone membrane with unidirectionally compliant electrodes on each side as described in [10]. Inspired by the work done by Takehiro et. al. [11, 12], the DEAP film is wound into two cylinders, as sketched in figure 1(b), attached to a diaphragm in a push-pull configuration (the assembled transducer is shown in figure 1(a)). Besides allowing the two DEAP cylinders to act in unison respectively pushing and pulling the diaphragm, the configuration inherently enables mechanically prestraining the elements. For simplicity, the following theory will be derived for a single wound DEAP cylinder.

The DEAP transducer is generally nonlinear as the electrostatic pressure, causing the strain of the transducer, increases with the square of the applied absolute voltage, $V_{Bias} + v(t)$

$$\sigma(t) \quad = \quad \varepsilon_0 \varepsilon_r \left(\frac{V_{Bias} + v(t)}{h} \right)^2, \tag{1}$$

with ε_0 being the permittivity of vacuum, ε_r, the relative permittivity of the dielectric material and h the distance between the electrodes [13, 10, 9]. The absolute voltage is separated into a static bias voltage V_{Bias} and a time dependent signal voltage $v(t)$. The nonlinear elongation is related to the absolute voltage across the electrodes, hence it is possible to reduce the nonlinear behavior by overlaying a large bias voltage with a smaller time dependent signal voltage, as shown in [14]. Assuming this condition to be met, the electrical and mechanical relationships of such a DEAP transducer can be approximated with a linear small-signal model. This section covers the displacement dependence of both capacitance and compliance of the DEAP transducer, while the detailed derivation of the small-signal model is described in the appendix.

Assuming the polymer of the DEAP film to be incompressible, the capacitance of a sheet of DEAP film can be expressed

$$C_{E0V} = \varepsilon_r \varepsilon_0 \frac{Area}{h_0} = \varepsilon_r \varepsilon_0 \frac{Vol}{h_0^2}, \tag{2}$$

with Vol being the volume of the dielectric material, $Area$ the electrode surface area, and h_0 the distance between the electrodes when the film is not deformed.

The capacitance of the DEAP transducer changes with the strain, ε

$$C_E = C_{E0V}(1+\varepsilon)^{k_A} = C_{E0V}\left(\frac{l_0+l(t)}{d}\right)^{k_A}, \tag{3}$$

where l_0 is the static length of the transducer, d the undeformed length, $l(t)$ is the time dependent length variation, and k_A is the degree of anisotropy. For a prestrain below 10 %, the change in compliance can be neglected [15], hence it can be included as part of the static length.

Neglecting geometrical effects due to winding the DEAP film into a cylinder, the compliance of the cylindrical DEAP transducer is given as

$$C_M = \frac{d}{YA_0}, \tag{4}$$

with Y being the Youngs modulus, and A_0 the cross sectional area of the undeformed transducer, as indicated in figure 1(b).

3. ANALYSIS

With the definitions and assumptions introduced in the theory, relating the strain to both capacitance and compliance, it is possible to define charge and energy balances, as seen in the appendix, to derive the small-signal model of the DEAP cylinder. It is shown, that two linear equations in two unknowns can be formulated to describe the coupling between the electrical and mechanical domain for the single DEAP cylinder. These are

$$v(\omega) = \frac{i(\omega)}{j\omega C_{E0V}}\left(\frac{l_0}{d}\right)^{-k_A} - \frac{V_{Bias}k_A u(\omega)}{j\omega l_0} \tag{5}$$

and

$$f(\omega) = \frac{k_A V_{Bias}}{j\omega l_0} i(\omega) - \frac{u(\omega)}{j\omega C_{M_{Eq}}}, \tag{6}$$

where $j = \sqrt{-1}$ and ω is the angular frequency. The frequency dependent voltage across the DEAP electrodes $v(\omega)$ is, in equation (5), related to the current flowing through the DEAP cylinder and voltage contribution due to the frequency dependent velocity of the diaphragm attached to the cylinder $u(\omega)$. In equation (6), the forces acting in the DEAP cylinder are related to the electrical attraction between the electrodes (dependent on $i(\omega)$) and the strain of the DEAP cylinder with an equivalent compliance $C_{M_{Eq}}$ at a given bias voltage and mechanical prestrain.

Combining equation (5) and equation (6) allows for the establishment of a fully coupled model from the electrical to the mechanical domain of the DEAP cylinder. The analogous circuit model is shown in figure 2. The model includes the electrical capacitance and mechanical compliance. These two components are coupled through current dependent voltage sources. For simpler notation the mechanical load on the system, besides the equivalent compliance, is denoted Z_M. This mechanical load is generally dominated by the moving mass of the system, but also includes the viscous losses and acoustical interactions affecting the mechanical system.

The transducer under investigation in this paper is a push-pull configuration utilizing two of the DEAP cylinders, whose lumped parameter models are drawn in figure 2. In the push-pull loudspeaker the two DEAP cylinders are combined to form a single transducer, with a corresponding model depicted in figure 3. This transducer is a device with three electrical terminals and two DEAP cylinders working in unison to displace the common diaphragm. However, for the investigations described in this paper, the bias and signal voltage was only applied to one of the two cylinders. As the coupling between

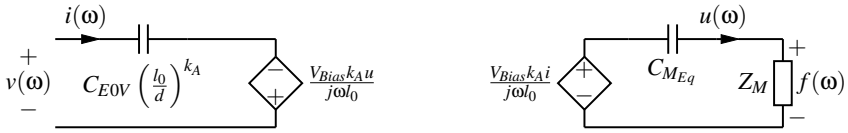


Figure 2: *DEAP transducer small signal model.*

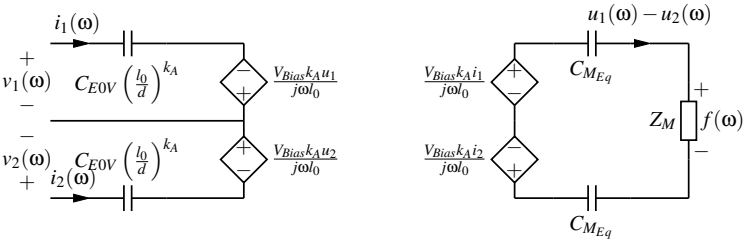


Figure 3: *Push-pull DEAP transducer small signal model.*

mechanical and electrical domains is proportional to the bias voltage, the effect of the added, inactive, element is regarded purely as an altered mass and compliance in the single cylinder model figure 2.

The input impedance of the analogous circuit model in figure 2 is

$$Z_{In} = \left(\frac{1}{j\omega C_{E0V}} \left(\frac{l_0}{d}\right)^{-k_A} - \frac{V_{Bias}^2 k_A^2}{(j\omega)^2 l_o^2 \left(Z_M + \frac{1}{j\omega C_{M_{Eq}}}\right)} \right) \tag{7}$$

Equation 7 consists of two terms: The first is the static capacitance at a certain static strain due to mechanical prestrain and bias voltage. The second term relates the harmonic displacement to the input impedance, scaled through the bias voltage amongst others. This term will cause the mechanical resonance to appear in the electrical impedance as the bias voltage is increased. The small-signal model introduced in this section does not include the effect of altered geometries nor complex vibrational modes. Hence, the model cannot be relied on above the first mechanical resonance where such artifacts are expected to occur.

Table 1: *Parameters of the push-pull loudspeaker*

	Designator	Value
Biasing voltage	V_{Bias}	0 –1.4 kV
Constant	k_A	2
Young's modulus	Y	2 MPa
Relative permittivity		3
Vacuum permittivity		8.854 $\frac{pF}{m}$
Average film thickness	h_0	40 μm
Length of un-rolled DEAP	b	3 m
Active height of DEAP cylinder	d	2 cm
Compliance	C_M	83.3 $\frac{\mu m}{N}$
Capacitance at 5 % prestrain	C_{E0V}	58.3 nF
Moving mass	L_M	15 g
Mechnical damping resistance	R_M	20 $\frac{Ns}{m}$

4. EXPERIMENTAL RESULTS

In order to characterize the DEAP transducer, its input impedance is measured with a biasing source connected to the transducer. The measuring setup used for this papers is shown in figure 4. A frequency response analyzer, AP300, from Ridley Engineering connected to an isolation transformer couples the test signal to the DEAP transducer. A Matsusada AU-5R60 high voltage supply ensures the bias voltage, with the $R_{Bias}C_{Bias}$ circuit providing a low impedance return path for the test signal. For the measurements $C_{Bias} = 10C_{E0V}$, $R_{Bias} = 1M\Omega$ and $R_{Sense} = 10\Omega$. A 1/200 differential probe was used to measure the voltage $v_{Out} + v_{Sense}$. An alternative measuring setup is proposed in [16] using a capacitive balanced bridge to measure the motional current of the DEAP transducer. The motional current is defined as the current trough the controlled voltage source(s) at the electrical side of figure 2 and figure 3. This measuring setup is proposed by Peter Walker for characterization of the electrostatic loudspeaker [16]. The setup relies on a capacitive balanced bridge, and is highly sensitive to components tolerances, making it unsuitable for most practical applications. Accordingly, this approach is disregarded.

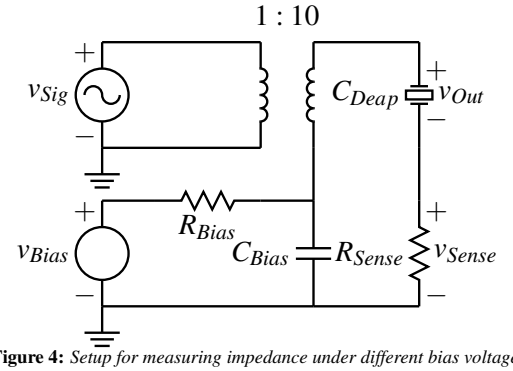


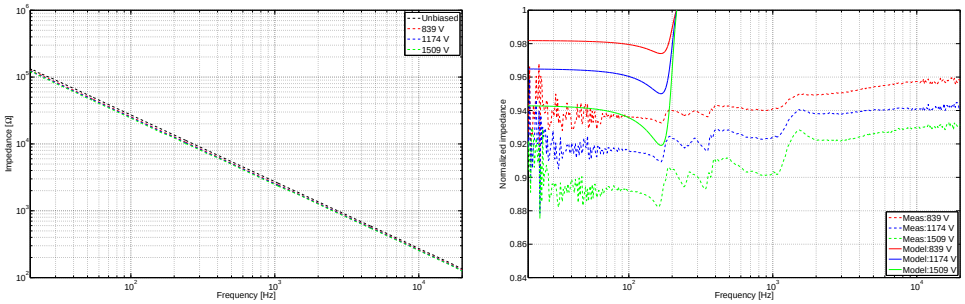
Figure 4: *Setup for measuring impedance under different bias voltages.*

Measurements are presented on the push-pull DEAP transducers based loudspeaker in figure 1(a). The push-pull loudspeaker is characterized using a 5 % pre-strain. During the measurements the bottom DEAP element is left as an open circuit, while the measuring circuit of figure 4 is connected to the top DEAP element. It is assumed, that symmetry applies and it is not within the scope of the paper to investigate any mismatch in the elements. Figure 5(a) gives the measured impedance for a selection of bias voltages. Notice that the input impedance is almost exclusively capacitive, and that the log-log plot only reveals the small change in the static capacitance. In order to make the effects of the bias voltage visible, the measured impedance at a given biasing voltage is normalized with the unbiased measured impedance, as shown in figure 5(b). Plotting the results on a linear y-axis shows, that the biasing voltage does indeed influence the impedance of the DEAP transducer. According to equation 3 the static capacitance should increase with the strain of the material. This is seen in figure 5(b), where the static capacitance dominates the impedance from 100 Hz and below. Another key observation is the mechanical resonances. The push-pull DEAP loudspeaker has its first mechanical resonance at 160 Hz. As the biasing voltage is increased this resonance peak becomes increasingly visible in the electrical domain. This is in accordance with equation (7).

Figure 5(b) shows significant noise at frequencies below 100 Hz. This is due to the limited bandwidth used for the measurements (10 Hz), and poor signal to noise ratio at these very low currents. Better signal to noise ratio can be achieved by increasing R_{Sense}. This is however at the expense of the bandwidth of the measuring setup.

5. DISCUSSION

The calculated normalized impedances using equation (7) are plotted in figure 5(b) for the parameters of Table 1. It is seen, that the model predicts the change in static impedance within 10 %, while taken into account the first resonance of the DEAP structure. Note that parameter tolerances of DEAP transducers is not a well-documented area, however [17] reports



(a) Impedance. (b) Normalized impedance.

Figure 5: *Impedance measurements of push-pull loudspeaker.*

of a 4 % spread in resonance frequency over 3 samples from the same production run. Especially the estimated moving or active mass is a rough estimate, assuming that half of the DEAP mass is moving [17]. Finite element analysis can be used to determine the actual moving mass, but this is beyond the scope of this paper. The model suggested in this paper, relies on Hooke's law for modeling the compliance of the DEAP transducer. Greater accuracy could be achieved by instead using the Mooney-Rivling equation for the compliance of the DEAP actuator [18]. It is proposed in [19] to model a tubular DEAP transducer using the modified Mooney-Rivlin equation. The modification is achieved by introducing a hardening factor taken into account the thickness and electrode properties. Also the coupling between the acoustical and mechanical domains can be included. This subject is, however well documented in the literature [8], and the influence is expected to be negligible due to a large box in which the DEAP transducer was mounted, ensuring the compliance of the system to be dominated by the transducer.

The complexity of the model can be increased in the pursuit of greater accuracy in numerous ways. Nevertheless the work of this paper documents, that the DEAP transducers based loudspeaker is to be considered as an almost exclusively capacitive load. However, as the material properties of the DEAP improves, and the thickness of the dielectric material is reduced, the model should be revisited with the new electrical and mechanical parameters, in order to verify that this conclusion is still valid.

6. CONCLUSION

This paper has derived the small-signal model of the DEAP transducer. Impedance measurements are used to validate the model. A measuring setup is proposed allowing for the DEAP impedance to be recorded under different biasing voltages. The experimental work is preformed on a push-pull DEAP transducer based loudspeaker. It is shown, that the model predicts the change in static impedance within 10 %, while taken into account the first resonance of the DEAP structure.

7. APPENDIX

This section derives the linearized small-signal model of the DEAP cylinder. Charge and energy balance equations are utilized to derive a set of linear coupled equations (two equations in two unkown).

7.1 Electrical charge

Using equation (3), the capacitance can be related to a the strain of the DEAP cylinder, depicted as part of figure 1(b). The total voltage related to the total charge is

$$V_{Bias} + v(t) = \frac{Q + q(t)}{C_E} \tag{8}$$

$$= \frac{Q + q(t)}{C_{E0V}} \left(\frac{l_0 + l(t)}{d} \right)^{-k_A}, \tag{9}$$

with Q being the static charge at a bias voltage, $q(t)$ the time dependent charge, and $v(t)$ the time dependent voltage. First order taylor expansion around $l(t) = 0$ and neglecting cross terms yields

$$V_{Bias} + v(t) = \frac{Q}{C_{E0V}} \left(\frac{l_0}{d}\right)^{-k_A} - \frac{k_A Q}{d C_{E0V}} \left(\frac{l_0}{d}\right)^{-k_A - 1} l(t) + \frac{q(t)}{C_{E0V}} \left(\frac{l_0}{d}\right)^{-k_A}. \quad (10)$$

Substituting $V_{Bias} = \frac{Q}{C_{E0V}} \left(\frac{l_0}{d}\right)^{-k_A}$ equation (10) becomes

$$v(t) = \frac{q(t)}{C_{E0V}} \left(\frac{l_0}{d}\right)^{-k_A} - \frac{V_{Bias} k_A l(t)}{l_0}. \quad (11)$$

Assuming linear and harmonic signals ($q(\omega) = \frac{i(\omega)}{j\omega}$ and $l(\omega) = \frac{u(\omega)}{j\omega}$) the equation can be written as

$$v(\omega) = \frac{i(\omega)}{j\omega C_{E0V}} \left(\frac{l_0}{d}\right)^{-k_A} - \frac{V_{Bias} k_A u(\omega)}{j\omega l_0}, \quad (12)$$

where $i(\omega)$ is the current through the static capacitance, and $u(\omega)$ is the velocity in the direction of the strain.

7.2 Energy

The total energy of the system is a sum of the electrical and mechanical energy

$$W = \frac{1}{2} \frac{(Q + q(t))^2}{C_E} + \frac{1}{2} \frac{(l_0 + l(t) - d)^2}{C_M}. \quad (13)$$

Using $V_{Bias} = \frac{Q}{C_{E0V}} \left(\frac{l_0}{d}\right)^{-k_A}$ the total energy is written as

$$W = \frac{1}{2} \frac{(Q + q(t))^2}{C_{E0V}} \left(\frac{l_0}{d}\right)^{-k_A} + \frac{1}{2} \frac{(l_0 + l(t) - d)^2}{C_M}. \quad (14)$$

The net force is found using the principal of virtual work, $f = -\frac{dW}{dl(t)}$. The time dependent force output of the DEAP cylinder is

$$f(t) = \frac{k_A (Q + q(t))^2}{2 d C_{E0V}} \left(\frac{l_0 + l(t)}{d}\right)^{-k_A - 1} - \frac{l_0 + l(t) - d}{C_M}. \quad (15)$$

Taylor expansion around $l(t) = 0$, and neglecting cross terms yields

$$\begin{aligned} f(t) &= \frac{k_A Q^2}{2 d C_{E0V}} \left(\frac{l_0}{d}\right)^{-k_A - 1} - \frac{l_0 - d}{C_M} + \frac{k_A Q q(t)}{d C_{E0V}} \left(\frac{l_0}{d}\right)^{-k_A - 1} \\ &- \frac{l(t)}{C_M} - \frac{k_A (k_A + 1) Q^2}{2 d^2 C_{EVO}} \left(\frac{l_0}{d}\right)^{-k_A - 2} l(t). \end{aligned} \quad (16)$$

The first and second term on the right hand side of the equation are the quiescent electrostatic force and the quiescent mechanical restoring force, which are equal but of opposite direction and thus cancels each other. Introducing $V_{Bias} = \frac{Q}{C_{E0V}} \left(\frac{l_0}{d}\right)^{-k_A}$, $q(\omega) = \frac{i(\omega)}{j\omega}$ and $l(\omega) = \frac{u(\omega)}{j\omega}$ yields

$$f(\omega) = \frac{k_A V_{Bias}}{j\omega l_0} i(\omega) - \frac{u(\omega)}{j\omega} \left(\frac{1}{C_M} + \frac{k_A (k_A + 1) V_{Bias}^2 C_{EVO}}{2 l_0^2} \left(\frac{l_0}{d}\right)^{k_A}\right). \quad (17)$$

The equivalent mechanical compliance is defined as

$$C_{M_{Eq}} = \frac{1}{\frac{1}{C_M} + \frac{k_A(k_A+1)V_{Bias}^2 C_{EVO}}{2l_0^2}\left(\frac{l_0}{d}\right)^{k_A}}. \tag{18}$$

Substituion equation (18) into equation (17) yields

$$f(\omega) = \frac{k_A V_{Bias}}{j\omega l_0} i(\omega) - \frac{u(\omega)}{j\omega C_{M_{Eq}}}. \tag{19}$$

In order to calculate l_0 at a given V_{Bias}, the problem of static elongation must be solved. The quiescent electrostatic and mechanical forces in equation (16) combine to describe the equilibrium

$$0 = \frac{k_A Q^2}{2dC_{E0V}}\left(\frac{l_0}{d}\right)^{-k_A-1} - \frac{l_0-d}{C_M}. \tag{20}$$

In the presence of a mechanical prestrain, without a bias voltage added to the opposing DEAP element this can be written

$$0 = \frac{k_A Q^2}{2dC_{E0V}}\left(\frac{l_0}{d}\right)^{-k_A-1} - \frac{l_0-d}{C_M} + \frac{l_{0_{opp}}-d}{C_M} \tag{21}$$

where the last term represents the force of the opposing DEAP cylinder. Assuming the DEAP cylinders are not compressed in the prestrain direction, the combined length of the transducer is

$$l_0 + l_{0_{opp}} = 2d(1+pre), \tag{22}$$

with pre being the prestrain. $V_{Bias} = \frac{Q}{C_{E0V}}\left(\frac{l_0}{d}\right)^{-k_A}$, equation (21) and equation (22) can be combined to

$$\frac{2l_0\,(2l_0 - 2d(1+pre))}{V_{Bias}^2 k_A C_M C_{E0V}} = \left(\frac{l_0}{d}\right)^{k_A}. \tag{23}$$

Linearization by taylor expansion around $l_0 = d$ yields

$$0 = l_0^2 \frac{4}{k_A V_{Bias}^2 C_{E0V} C_M} + l_0\left(\frac{-4d(1+pre)}{k_A V_{Bias}^2 C_{E0V} C_M} - \frac{k_A}{d}\right) + k_A - 1. \tag{24}$$

Equation (24) is a second order equation, and can be solved for l_0. Note, that $d \leq l_0$.

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Dennis Nielsen, Arnold Knott and Michael A. E. Andersen, "Hysteretic self-oscillating bandpass current mode control for class D audio amplifiers driving capacitive transducers", ECCE Asia Downunder (ECCE Asia), 2013.

Hysteretic self-oscillating bandpass current mode control for Class D audio amplifiers driving capacitive transducers

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***Abstract*—A hysteretic self-oscillating bandpass current mode control (BPCM) scheme for Class D audio amplifiers driving capacitive transducers are presented. The scheme provides excellent stability margins and low distortion over a wide range of operating conditions. Small-signal behavior of the amplifier is analysis through transfer function based linear control methodology. Measurements are performed on a single-ended $\pm$ 300 V half-bridge amplifier driving a capacitive load of 100 nF. Total Harmonic Distortion plus noise (THD+N) below 0.1 % are reported. Transducers representing a capacitive load and obeying the rules of electrostatics have been known as very interesting alternatives to the traditional inefficient electrodynamic transducers. When driving capacitive transducers from a Class D audio amplifier the high impedance nature of the load represents a key challenge. The BPCM control scheme ensures a flat frequency response (within 3 db) over the midrange region of 200 Hz – 3.5 kHz.**

I. Introduction

Switch-mode audio power amplifiers are commonly used in sound reproduction driving electrodynamic transducers. While these audio systems are dominating the market of sound reproduction, they suffer from the poor efficiency imposed by the electrodynamic transducer. As a consequence the audio community is constantly searching for new high efficient audio transducers. An alternative to the electrodynamic transducer is the electrostatic transducer. Electrostatic transducers are known from their usage in electrostatic loudspeakers, however Dielectric Electro Active Polymers (DEAP) can also be used to form an electrostatic transducer. Such capacitive transducers present a high impedance, frequency depended nonlinear load to the amplifier. A DEAP transducer is shown in figure 1. Commercial electrostatic loudspeakers are driven from tube, linear or audio-transformer based amplifier solutions. Consequently these systems suffer from being bulky, fragile and inefficient. In order to establish the full potential of the electrostatic transducer, a new generation of audio amplifiers must be developed. These amplifiers should have a high power density, low power loss and be robust. Accordingly it is proposed to use a switch-mode audio amplifier or class D amplifier for driving the electrostatic transducer. Switch mode audio amplifiers are known for their low power consumption, high power density and excellent audio figures (for instance low Total Harmonic Distortion or THD) [1], [2], [3], [4]. This paper presents a hysteretic based self-oscillating bandpass current mode control scheme for Class D audio amplifiers driving capacitive transducers. Class D audio amplifiers driving capacitive loads and their control loop is an area of research with little to no publications.

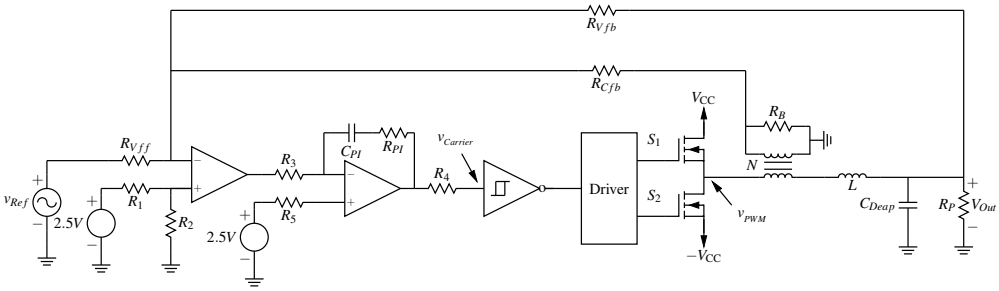
Figure 1: DEAP transducer.

II. Theory

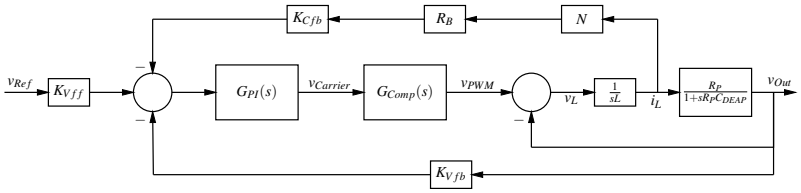
This section introduces the fundamental idea of the bandpass current mode control (BPCM) control scheme, and describes the small-signal model used for the analysis and design process.

A. Bandpass Current Mode Control

BPCM control schemes for Class D audio amplifiers driving electrodynamic transducers are well-known [5], [1], [6], [7], [8]. The big advantage of such control schemes is the fact, that stability is maintained, even when no load is connected to the amplifier. As a consequence the zobel network used to damp the high Q of an unloaded amplifier can be eliminated



(a) Schematic with single-supply control circuitry.



(b) Small-signal model.

Figure 2: Class D amplifier with BPCM control.

[5]. When driving a capacitive transducer, it will be a natural choice to use the transducer as the output filter capacitor of the half-bridge converter. The half-bridge converter constitutes a very typical way of implementing a Class D amplifier. Consequently a second order LC output filter with no damping is created. The damping can be implemented either with an active or passive approach. This paper uses active damping, as losses will be unacceptably high in passive damping configurations. Active damping is essentially what the BPCM scheme ensures by letting the output filter inductor act as a current source around the resonance frequency of the output filter. Implementation of the BPCM scheme is achieved by either direct measurement or estimation of the inductor current [9], [10]. For this application the inductor current is measured using a current sense transformer. Accordingly an isolated feedback signal with enough bandwidth to handle the switching frequency is obtained. Figure 2(a) shows a schematic of the Class D amplifier with BPCM control scheme, while figure 2(b) gives the small-signal model of the amplifier. The closed-loop transfer function of the inner loop, denoted as the bandpass current mode loop, is

$$G_{BPCM,cl}(s) = \frac{G_{PI}(s)G_{Comp}(s)}{1+s\frac{L}{R_P}+s^2C_{DEAP}L+K_{Cfb}G_{PI}(s)G_{Comp}(s)R_{Sense}N\frac{1+R_PC_{DEAP}s}{R_P}} \quad (1)$$

with $G_{Comp}(s)$ being the small-signal transfer function of the hysteresis comparator and power stage, $G_{PI}(s)$ the transfer function of the PI regulator and R_P the parallel resistance of the capacitive transducer.

The open-loop transfer function of the complete amplifier is

$$G_{Tot,ol}(s) = K_{Vfb}G_{BPCM,cl}(s) \quad (2)$$

while the closed-loop transfer function of the complete amplifier is defined as

$$G_{Tot,cl}(s) = \frac{K_{Vff}G_{BPCM,cl}(s)}{1+G_{Tot,ol}(s)} \quad (3)$$

For the purpose of designing the self-oscilation control loop, the controller transfer function must be defined

$$G_{Ctrl}(s) = \frac{v_{Carrier}(s)}{v_{PWM}(s)} \quad (4)$$

$$= G_{PI}(s)\left(K_{Vfb}+K_{Cfb}R_{Sense}N\frac{1+R_PC_{DEAP}s}{R_P}\right)\frac{1}{LC_{DEAP}s^2+\frac{L}{R_P}s+1} \quad (5)$$

III. Analysis

A. Closed-loop response

Referring to equation (1), the term $1+sR_PC_{DEAP}$ will for all practical values have its cut-off frequency below the audio bandwidth, and because the parallel capacitance of the DEAP, R_P, is consider infinite large, equation (1) is simplified to

$$G_{BPCM,cl}(s) = \frac{G_{PI}(s)G_{Comp}(s)}{1+s^2C_{DEAP}L+K_{Cfb}G_{PI}(s)G_{Comp}(s)R_{Sense}NC_{DEAP}s} \quad (6)$$

For the purpose of evaluating the closed-loop response of the amplifier, G_{PI} will be assumed equal to unity and $G_{Comp}(s)$ will be considered as an infinity gain. Equation (6) the becomes

$$G_{BPCM,cl}(s) = \frac{1}{K_{Cfb}R_{Sense}NC_{DEAP}s} \quad (7)$$

From 7 is it seen, that the closed-loop response of the BPCM loop is a pure integrator. The closed-loop response of the complete amplifier then becomes

$$G_{Tot,cl}(s) = \frac{K_{Vff}\frac{1}{K_{Cfb}R_{Sense}NC_{DEAP}s}}{1+\frac{1}{K_{Cfb}R_{Sense}NC_{DEAP}s}K_{Vfb}} \quad (8)$$

$$= \frac{K_{Vff}}{K_{Cfb}R_{Sense}NC_{DEAP}s+K_{Vfb}} \quad (9)$$

Accordingly, the closed-loop response of the amplifier is a first order low pass with cut-off frequency of $\frac{K_{Cfb}R_{Sense}NC_{DEAP}}{K_{Vfb}}$ and DC-gain of $\frac{K_{Vff}}{K_{Vfb}}$.

B. Self-oscillation

Oscillation is ensured by shaping the open-loop frequency response to have a phase shift of 360 ^{o} and unity gain at the targeted switching frequency. This is the Barkhausen Oscillation criterium. It can be shown, that the switching frequency is described by the function [11], [5]

$$f_{Sw}(D) = \frac{D(1-D)}{2\frac{V_{Hyst}}{K}+t_D} \quad (10)$$

With K defined as:

$$K = 2V_S \times step\{\lim_{s\to\infty} G_{Ctrl}(s)\} \quad (11)$$

Assuming G_{PI} has no influence on the switching frequency, K can be derived using equation (11) and (5)

$$K = \frac{2V_S K_{Cfb}NR_{Sense}}{L} \quad (12)$$

The concept of carrier linearization is introduced in [5]. It can be shown, that the optimal carrier of the amplifier in figure 2 is achieved, if

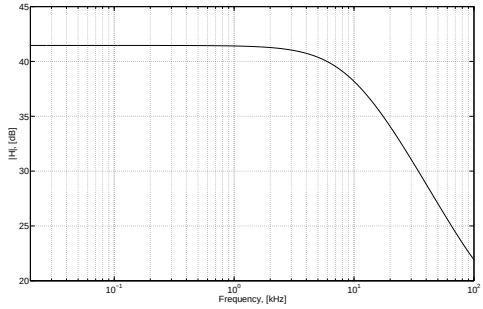
$$\frac{K_{Vfb}L}{C_{DEAP}} = K_{Cfb}NR_{Sense}^2 \quad (13)$$

IV. Calculations

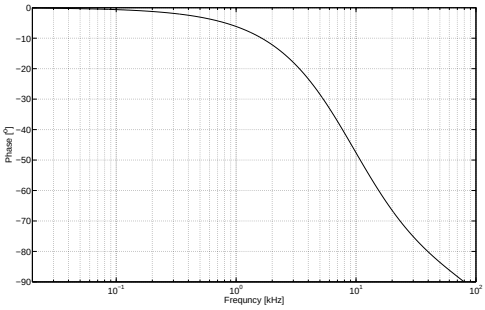
Using the equations of section II and III, the design parameters of table I can be derived. The corresponding closed-loop response of the amplifier are shown in figure 3 (equation 3). Notice how the response is flat (within 3 db) over the midrange region of 200 Hz – 3.5 kHz.

Table I: Design parameters

	Designator	Value
Idle switching frequency	f_{Sw}	300 kHz
Output filter inductance	L	200 uH
DEAP Capacitance	C_{DEAP}	100 nF
Supply voltage	$\pm$ V_{CC}	$\pm$ 300 V
Output filter resonance filter	f_r	35.6 kHz
Closed-loop gain	A_V	43.5 dB
Loop time delay	t_D	250 ns
Hysteresis window	v_{Hyst}	720 mV



(a) Magnitude of small-signal closed-loop frequency response.



(b) Phase of small-signal closed-loop frequency response.

Figure 3: Calculated closed-loop BPCM response.

Table II: Component values

Component	Value
R_B	100 Ω
C_{PI}	3 nF
R_{PI}	1 $k\Omega$
R_{Cbf}	2 $k\Omega$
R_{Vff}	2 $k\Omega$
R_{Vfb}	300 $k\Omega$
N	$\sqrt{\frac{200nH}{980uH}} \approx 0.014$

V. Measurements

Figure 4 shows the prototype amplifier, which is based on a Si8235 digital isolated gate driver and SPA08N80C3 MOSFET's. The BPCM control scheme are implemented using a single-supply control circuitry with a THS4221 comparator and LVM7219 operation amplifiers. Current measurement is preformed using the current sense transformer, CST1-070LB, of Coilcraft. A polypropylene capacitor is used as dummy load to perform all measurements. Table II shows the key component values of the prototype amplifier.

Figure 5 shows the reference, switching node and output voltages, when operating with a reference frequency of 1 kHz

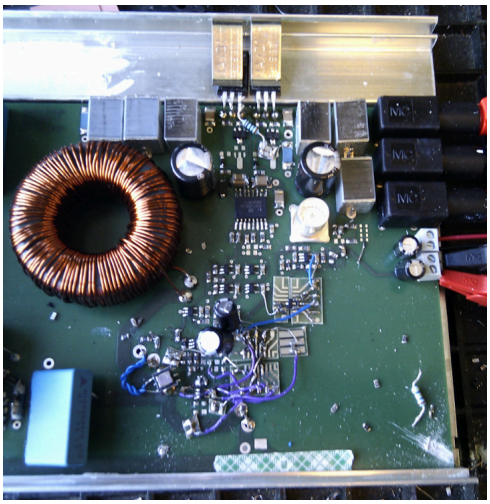


Figure 4: Prototype amplifier.

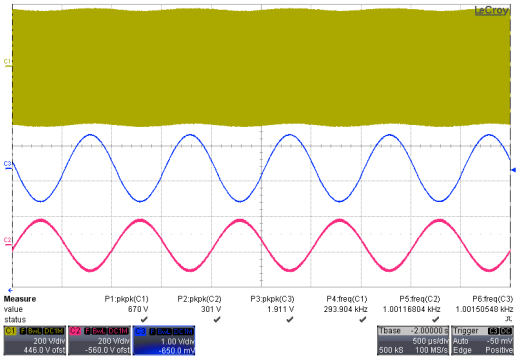


Figure 5: Waveforms of prototype amplifier.

and output voltage of 150 V amplitude (modulation index of 0.5). The carrier are given in figure 6 under idle operation. An idle switching frequency of 294 kHz is observed. This is acceptably close to the targeted 300 kHz.

A. THD+N

THD+N is measured using an APX525 audio analyzer and a voltage attenuation interface. The voltage attenuation interface is necessary in order to protect the input of the audio analyzer. Design and implementation of the voltage attenuation interface is well-described in the literature [12], [13], and will not be part of this paper. Figure 7 gives the measured THD+N as function of the reference voltage for the frequencies of 100 Hz and 1 kHz. The THD+N is below 0.1% over a significant part of the operation range.

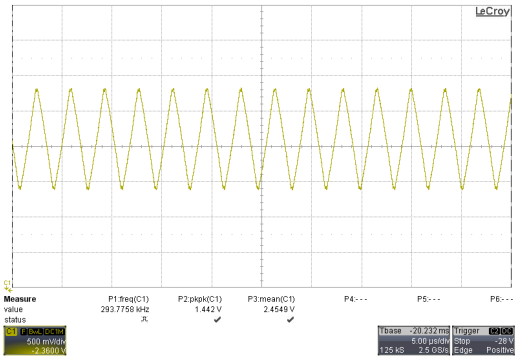


Figure 6: Carrier waveform.

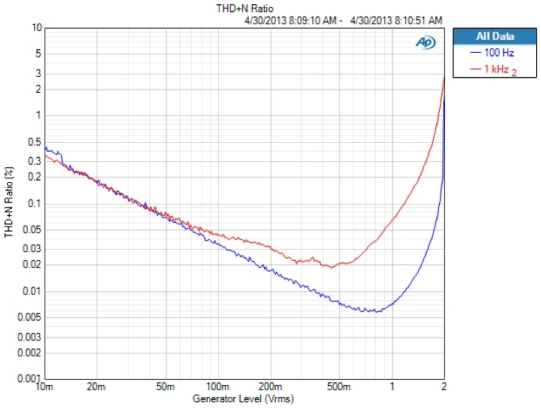


Figure 7: THD+N (100 Hz and 1 kHz).

B. Closed-loop frequency response

The voltage attenuation interface and the APX525 audio analyzer are also used to measure the closed-loop frequency response. Figure 8 gives the small-signal frequency response. The response is flat (within 3 dB) over the midrange region of 200 Hz – 3.5 kHz, showing that the active damping have been successfully implemented.

VI. Conclusion

A hysteretic self-oscillating bandpass current mode control scheme for Class D audio amplifiers driving capacitive transducers is presented, analyzed and evaluated. THD+N of typically 0.1 % are shown. Design guidelines are given, and it is shown that active damping can be implemented successfully using the bandpass current mode control scheme. Measurements are performed on a single-ended $\pm$ 300 V half-bridge amplifier driving a capacitive load of 100 nF. The closed-loop frequency response of the prototype amplifier is shown to be flat (within 3 db) over the midrange region of 200 Hz – 3.5 kHz.

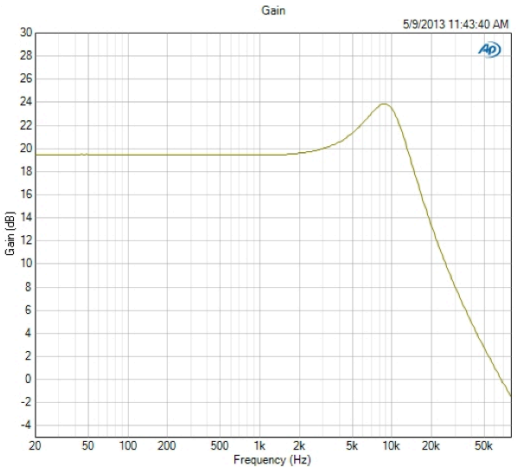


Figure 8: Closed-loop response of the prototype amplifier. Notice when comparing with figure 3, that the voltage attenuation interface has a gain of - 23 dB.

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Dennis Nielsen, Arnold Knott and Michael A. E. Andersen, "A high-voltage class D audio amplifier for dielectric elastomer transducers", Applied Power Electronics Conference and Exposition (APEC), 2014.

A High-Voltage Class D Audio Amplifier for Dielectric Elastomer Transducers

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***Abstract*— Dielectric Elastomer (DE) transducers have emerged as a very interesting alternative to the traditional electrodynamic transducer. Lightweight, small size and high maneuverability are some of the key features of the DE transducer. An amplifier for the DE transducer suitable for audio applications is proposed and analyzed. The amplifier addresses the issue of a high impedance load, ensuring a linear response over the midrange region of the audio bandwidth (100 Hz – 3.5 kHz). THD+N below 0.1% are reported for the $\pm$ 300 V prototype amplifier producing a maximum of 125 Var at a peak efficiency of 95 %.**

INTRODUCTION

Class D audio amplifiers are commonly used in sound reproduction driving electrodynamic transducers [1], [2], [3], [4], [5], [6], [7]. While these audio systems are dominating the market of sound reproduction, they suffer from the poor efficiency imposed by the electrodynamic transducer, and the weight of the electromagnet. As a consequence the audio community is constantly searching for new audio transducers. An alternative to the electrodynamic transducer is the electrostatic transducer. Electrostatic transducers are known from their usage in electrostatic loudspeakers, however Dielectric Elastomers (DE) can also be used to form an electrostatic transducer [8], [9], [10]. Such capacitive transducers present a high impedance, frequency depended nonlinear load to the amplifier. A DE transducer is shown in figure 1. The DE transducer is constructed by printing compliant electrodes on a thin piece of silicone. Commercial electrostatic loudspeakers are driven from tube, linear or audio-transformer based amplifier solutions. Consequently these systems suffer from being bulky, fragile and inefficient. In order to establish the full potential of the DE transducer, a new generation of audio amplifiers must be developed. These amplifiers should have a high power density, low power loss and be robust. Accordingly it is proposed to use a switch-mode audio amplifier or class D amplifier for driving the DE transducer [11], [12]. Class D audio amplifiers are known for their low power consumption, high power density and excellent audio figures (for instance low Total Harmonic Distortion plus Noise or THD+N) [4], [13], [1], [2]. In this paper a half-bridge based class D amplifier is proposed as amplifier for the DE transducer. A hysteretic based self-oscillating bandpass current mode control scheme is suggested, ensuring high loop gain and thus excellent THD+N. It should be noted, that DE transducers and their amplifiers are not limited to the application of sound reproduction. Microrobotics with DE transducers is another application, which has recieved interest in recent years [14].

Fig. 1: DE actuator.

THEORY

When driving a DE transducer it is appropriate to give a formal definition of the term efficiency. The first order approximation will yield a capacitive load. Accordingly no real power will be delivered to the load. Efficiency will thus be defined as

$$\eta = \frac{P_{Out}}{P_{Out}+P_{In}} \tag{1}$$

where $P_{Out} = \frac{V_{rms}^2}{\left(\frac{1}{2\pi f_{Ref} C_{Deap}}\right)}$, the reactive power delivered to the load, and P_{In} corresponding to the real power consumed by the amplifier. This definition of the term efficiency will be used throughout the paper.

Losses

The paper analysis the power stage of figure 2. Notice, that the inductor current equals the current of C_{DE} ($i_L(t) = i_{C_{DE}}(t)$), because the parallel resistance of C_{DE}, R_P, has a value of 1 MΩ or above [10]. The current $i_L(t)$ is a superposition of the ripple ($\Delta i_L(D)$) and the sinusoidal reference or audio current ($i_{Ref}(t)$)

$$i_L(t) = \Delta i_L(D) + i_{Ref}(t) \tag{2}$$

The following definitions will be used

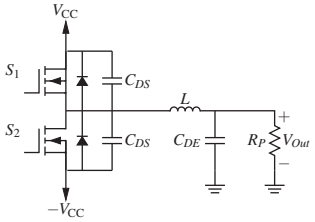


Fig. 2: Half-Bridge class D amplifier.

$$\Delta i_L(D) = \frac{1-D}{L} V_{CC} D T_{Sw} \tag{3}$$

The Root Mean Square (RMS) and Average (AV) value of 3 can be expressed as functions of the modulation index, M [15]. Using the relation $D(t) = \frac{1}{2}(Msin(2\pi f_{Ref} t) + 1)$ is can be shown that [15]

$$\Delta i_{L,RMS}(M) = \frac{V_{CC}}{4 L f_{Sw}} \sqrt{\frac{1-M^2}{3} + \frac{M^4}{8}} \tag{4}$$

The RMS value of the reference current is defined as

$$i_{Ref,RMS}(M) = \frac{V_{CC} M}{\sqrt{2}} 2\pi f_{Ref} C_{DE} \tag{5}$$

DE loss

The DE transducers is model as a capacitor with a series resistance, neglecting dielectric losses. Accordingly

$$P_{DE} = R_{Si} i^2_{L,rms} \tag{6}$$

Magnetic loss

The magnetic loss is divided into conduction and ferrite loss. Conduction losses are defined as

$$P_{Cu} = R_{Cu} i^2_{L,rms} \tag{7}$$

with

$$R_{Cu} = \frac{\rho N l_T}{A_{Wire}} \tag{8}$$

N is the number of turns, l_T the average length of a turn, A_{Wire} the wire cross-sectional area and ρ the resistivity. Only single layer winding schemes are considered.

Steinmetz equation are used to estimate the ferrite loss

$$P_{Fe} = V_{Core} k_{Fe} \left(\left(\frac{f_{Ref}}{f_0} \right)^{\alpha} \left(\frac{B(i_{Ref})}{B_0} \right)^{\beta} + \left(\frac{f_{Sw}}{f_0} \right)^{\alpha} \left(\frac{B(\Delta i_L(M))}{B_0} \right)^{\beta} \right) \tag{9}$$

Greater accuracy can be achieved by use of the improved Steinmetz equation. However, for the purpose of this paper Equation (9) is sufficient.

Semiconductor loss

The semiconductor losses are divided into conduction and switching losses. The conductions loss caused by the MOSFET on resistance, $R_{DS_{On}}$, is

$$P_{DS_{On}} = R_{DS_{On}} i^2_{L,rms} \tag{10}$$

The switching loss can be approximated by [16]

$$P_{Sw} = \begin{cases} 4 f_{Sw} C_{DS} V^2_{CC} & i_{Ref}(M) \le \Delta i_L(M) \\ f_{Sw} V_{CC} \tau(i_{Ref}) \frac{I_L}{\pi} + 4 f_{Sw} C_{DS} V^2_{CC} & i_{Ref}(M) > \Delta i_L(M) \end{cases} \tag{11}$$

with

$$\tau(I_L) = R_G Q_{GD} \left(\frac{1}{v_{GS,th} + \frac{I_L}{g}} + \frac{1}{V_G - v_{GS,th} - \frac{I_L}{g}} \right) \tag{12}$$

$$+ R_G C_{ISS} \ln \left(\frac{v_{GS,th} + \frac{I_L}{g}}{v_{GS,th}} \frac{V_G - v_{GS,th}}{V_G - v_{GS,th} - \frac{I_L}{g}} \right) \tag{13}$$

Zero voltage switching

Switching losses can be limited by ensuring soft switching or zero voltage switching (ZVS) of the MOSFETs. The quasi-square wave ZVS buck converter is analyzed in [17], and ZVS is guaranteed at 50 % duty cycle, if the switches are operated with sufficient deadtime. The deadtime can be evaluated as

$$t_{Dead} = \frac{\pi}{2} \sqrt{L C_{Sw}}. \tag{14}$$

The resonance tank of L and C_{Sw} reaches its maximum amplitude at $\frac{T}{4}$. T being the resonance period. C_{Sw} equals to two times the mosfet drain-source capacitance plus any other capacitive couplings at the switching node. The later includes coupling to the heatsink, the equivalent capacitance constructed from the output filter inductor parallel capacitance and C_{DEAP} etc.

Dead-time distortion

Several publications have analyzed the influence of pulse-timing errors on THD [18], [19], [16]. These are traditional divided into the categories of dead-time distortion, finite switching speed and conduction state errors. When operating the power stage at ZVS, the dead-time distortion becomes a key concern. It is shown in [16], that dead-time distortion is a function of the ratio between reference and ripple current. This section analyzes dead-time distortion for a class D amplifier driving a capacitive load. Voltage mode control is assumed, meaning that the output current no longer can be considered constant with respect to frequency. This is unlike the case of driving an electrodynamic loudspeaker, where the load typically is assumed being resistive, and those the output current does not change with frequency. Let the THD arising from dead-time distortion being defined as [16]

$$THD_d(M, \alpha_d, \alpha_I) = \frac{\Delta(\alpha_I) \sqrt{\sum_{i=2}^{N_{Max}} \left[2\alpha_d \frac{sin(i\frac{\pi}{2})}{i\frac{\pi}{2}} \right]^2}}{M - \alpha_d \frac{4}{\pi} \Delta(\alpha_I)}$$

where the dead-time delay factor is the ratio of the dead-time to the period of the switching frequency

$$\alpha_d = \frac{t_d}{T_{sw}} \tag{15}$$

and the ripple current factor

$$\alpha_I = \frac{\Delta i_L(M)}{i_{Ref}(M)} \tag{16}$$

The ripple current factor is the amplitude of the ripple current divided by the reference current. Both being functions of the modulation index, M.

Using the ripple current factor $\Delta(\alpha_I)$ of equation (15) is defined

$$\Delta(\alpha_I) = \begin{cases} 0 & i_{Ref}(M) \leq \Delta i_L(M) \\ \frac{\frac{\pi}{2} - arcsin(\alpha_I)}{\frac{\pi}{2}} & i_{Ref}(M) > \Delta i_L(M) \end{cases} \tag{17}$$

ANALYSIS

The following analysis assumes the basic design parameters of Table I. Using these parameters $\Delta i_L = 1.07A$. With a maximum output current of $300V2\pi3.5kHz100nF = 660mA$, the dead-time distortion does not compromise the overall THD even though the power stage is operated at ZVS.

TABLE I: Design parameters

	Designator	Value
Idle switching frequency	f_{Sw}	300 kHz
Output filter inductance	L	200 uH
DE Capacitance	C_{DE}	100 nF
Supply voltage	V_{CC}	$\pm$ 300 V
Closed-loop gain	A_V	43.5 dB
Loop time delay	t_D	250 ns
Hysteresis window	v_{Hyst}	720 mV
Bandwidth	f_{Ref}	100 Hz – 3.5 kHz

Parameters related to the losses are gathered in Table II. The output filter inductor is constructed using a T184-2 toroidal core from Micrometals, while the MOSFETs are of the type SPA08N80C3.

TABLE II: Parameters key to the loss analysis.

	Designator	Value
Drain-source on resistance	$R_{DS_{On}}$	650 mΩ
Drain-source capacitance	C_{DS}	16 pF
Number of inductor windings	N	92
DC resistance of output filter inductor	R_S	404mΩ

The individual loss components are plotted in figure 3 as function of the modulation index. Ferrite losses are the dominating ones.

IMPLEMENTATION

It is proposed to use a half-bridge power stage with hysteresis bandpass current mode control (BPCM), as amplifier for the DE transducer. BPCM control schemes for class D

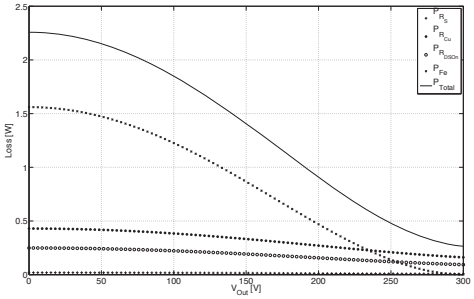


Fig. 3: Breakdown of losses.

audio amplifiers driving electrodynamic transducers are well-known [6], [4], [20], [5], [21]. The big advantage of such control schemes is the fact, that stability is maintained, even when no resistive load is connected to the amplifier. As a consequence the zobel network used to damp the high Q of an unloaded amplifier can be eliminated [6]. Implementation of the BPCM scheme is achieved by either direct measurement or estimation of the inductor current [22], [8]. For this application the inductor current is measured using a current sense transformer. Accordingly an isolated feedback signal with enough bandwidth to handle the switching frequency is obtained. Figure 4(a) shows a schematic of the Class D amplifier with BPCM control scheme, while figure 4(b) gives the small-signal model of the amplifier.

A. Self-oscillation

Oscillation is ensured by shaping the open-loop frequency response to have a phase shift of 360 ^{o} and unity gain at the targeted switching frequency. This is the Barkhausen Oscillation criterium. It can be shown, that the switching frequency is described by the function [7], [6]

$$f_{Sw}(D) = \frac{D(1-D)}{2\frac{V_{Hyst}}{K} + t_D} \tag{18}$$

With K defined as:

$$K = 2V_{CC} \times step\{\lim_{s\to\infty} G_{Ctrl}(s)\} \tag{19}$$

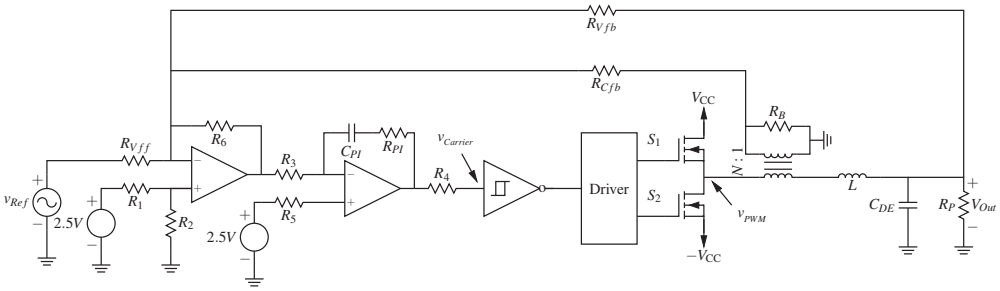
For the purpose of designing the self-oscilation control loop, the controller transfer function must be defined

$$G_{Ctrl}(s) = \frac{v_{Carrier}(s)}{v_{PWM}(s)} \tag{20}$$

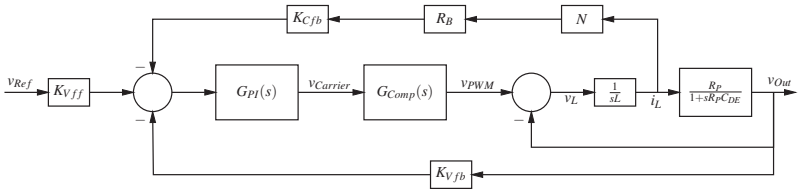
$$= G_{PI}(s)\left(K_{Vfb} + K_{Cfb}R_{Sense}N\frac{1+R_P C_{DEAP} s}{R_P}\right)\frac{1}{LC_{DEAP}s^2 + \frac{L}{R_P}s + 1} \tag{21}$$

K can be derived using equation (19) and (21)

$$K = \frac{2V_S K_{Cfb} N R_{Sense}}{L} \tag{22}$$



(a) Schematic with single-supply control circuitry.



(b) Small-signal model.

Fig. 4: Half-brigde amplifier with BPCM control.

TABLE III: Component values

Component	Value
R_B	100 Ω
C_{PI}	10 nF
R_{PI}	1 $k\Omega$
R_{Cbf}	2 $k\Omega$
R_{Vff}	2 $k\Omega$
R_{Vfb}	300 $k\Omega$
R_1, R_2, R_3, R_4, R_5 and R_6	1 $k\Omega$
N	$\sqrt{\frac{200nH}{980uH}} \approx 0.014$

Experimental results

A prototype amplifier has been constructed. The amplifier operates from ± 300 V delivering a maximum power of 125 Var to a 100 nF capacitive load. Figure 5 shows the prototype amplifier, which is based on a Si8235 digital isolated gate driver. The BPCM control scheme are implemented using a single-supply control circuitry with a THS4221 comparator and LVM7219 operation amplifiers. Current measurement is preformed using the current sense transformer, CST1-070LB, of Coilcraft. A polypropylene capacitor is used as dummy load to perform all measurements. Table III shows the key component values of the prototype amplifier.

Efficiency

The measured efficiency is given in figure 6. The efficiency is defined in accordance with equation 1, and measured using the WT1600 digital power analyzer form Yokogawa. Note, that the efficiency at 100 Hz is below 42 %. Because the output voltage is kept fixed with respect to frequency, the reactive output power will drop inversely proportional with frequency. At 100 Hz the switching loss becomes comparable with the reactive output power. An efficiency above 90 % is achieved for the reference frequency 3.5 kHz. Voltage mode control of electrostatic transducers is preferred for applications were displacement is of concern. Charge mode control ensures greater linearity at the expense of displacement [23].

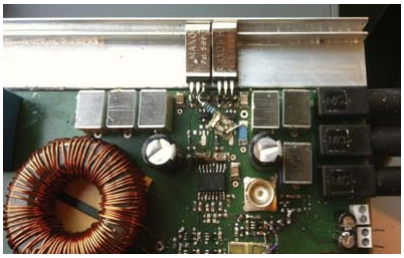


Fig. 5: Power stage used for the prototype amplifier.

THD+N and closed-loop response

THD+N is measured using an APX525 audio analyzer and a voltage attenuation interface. The voltage attenuation interface is necessary in order to protect the input-stage of the audio analyzer. Design and implementation of the voltage attenuation

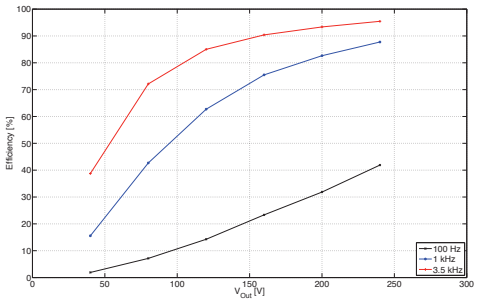
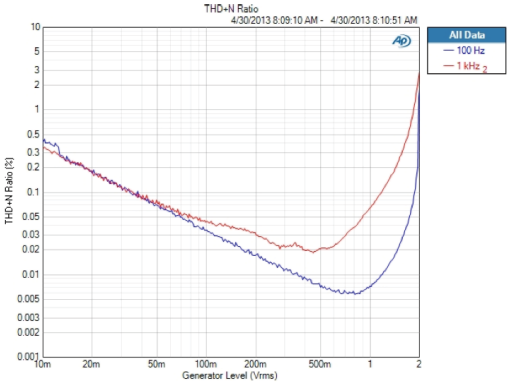
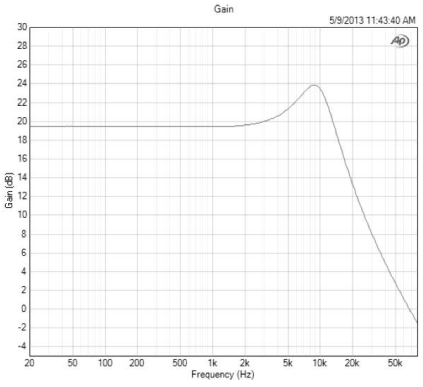


Fig. 6: Measured efficiency.



(a) THD+N for the reference frequencies of 100 Hz and 1 kHz.



(b) Small-signal closed-loop response.

Fig. 7: Measuring results of prototype amplifier.

interface is well-described in the literature [11], [24]. Figure 7(a) gives the measured THD+N as function of the reference voltage for the frequencies of 100 Hz and 1 kHz. THD+N is below 0.1% over a significant part of the operation range. Noise is the dominating factor in the measured THD+N. The measured small-signal closed-loop frequency response is given in Figure 7(b). The response is flat (within 3 dB) over the midrange region of 100 Hz – 3.5 kHz.

Conclusion

A class D audio amplifier for dielectric elastomer transducers is proposed and analyzed. The amplifier addresses the issue of a high impedance load, ensuring a linear response over the midrange region of the audio bandwidth (100 Hz – 3.5 kHz), potentially paving the way for increased industry adoption of the highly promising technology of dielectric elastomers. THD+N below 0.1% are reported for the $\pm$ 300 V prototype amplifier producing a maximum of 125 Var at a peak efficiency of 94 %.

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Multilevel inverter based class D audio amplifier for capacitive transducers

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Keywords

Multilevel converters, High voltage power converters, Drive, Active damping, Amplifiers

Abstract

The reduced semiconductor voltage stress makes the multilevel inverters especially interesting, when driving capacitive transducers for audio applications. A $\pm$ 300 V flying capacitor class D audio amplifier driving a 100 nF load in the midrange region of 0.1-3.5 kHz with Total Harmonic Distortion plus Noise (THD+N) below 1 % is presented.

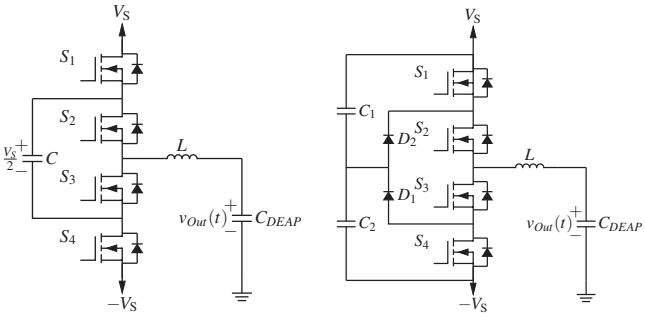
Introduction:

Class D audio amplifiers are commonly used in sound reproduction systems due to their superior cost, size and efficiency compared to their linear counterparts [1, 2]. While these audio systems are dominating the market of sound reproduction, they still suffer from the poor efficiency imposed by the electrodynamic transducer. An alternative to the electrodynamic transducer is the capacitive transducer. Capacitive transducers are most known from their usage in electrostatic loudspeakers, however Dielectric Electro Active Polymers (DEAP) can also be used to form a capacitive transducer [3, 4, 5]. With the goal of creating smaller, cheaper and more efficient audio systems it is proposed to use a class D amplifier as driver of the capacitive transducer [6, 7]. Class D amplifiers driving a capacitive transducer without the use of audio or high frequency linked transformers, is an area of research with little to no publications. This paper analyzes the use of multilevel inverters as power stages in class D audio amplifiers for capacitive transducers (Dielectric Electro Active Polymers (DEAP), electrostatic or piezoelectric loudspeakers).

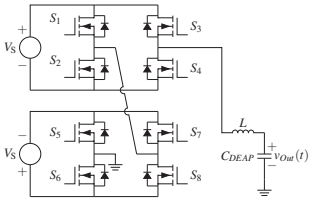
Class D audio amplifiers are traditional based around half- or full-bridge power stages [8, 9, 10]. The half-bridge power stage allows for two level modulation, while the full-bridge can be used for either two or three level modulation. Phase-shifting of multiple half-bridges have been proposed as a way of implementing higher modulation orders [11, 12, 13, 2]. All of these configurations are part of the power stages denoted as linear, because the output voltage is a linear function of the duty cycle. However, in the class of linear switching power stages one group has traditionally been neglected. These are the multilevel inverters, which have gained significant commercial success in other regions of power electronics (motor-drive systems and enveloped tracking) [14, 15, 16]. Multilevel inverters are in general more complex than their half or full-bridge counterparts. This is, among others, due to the high number of floating sources and extra boot-strap circuits needed to drive the floating MetalOxideSemiconductor Field-Effect Transistors (MOSFET's). Nevertheless multilevel inverters possess some very interesting properties. The semiconductor voltage stress is reduced as MOSFET's effectively are stacked with circuity ensuring proper voltage sharing [17]. Semiconductor voltage stress is not a key concern for class D amplifiers driving the low impedance of an electrodynamic loudspeaker. However capacitive transducers requires operation voltage ranging from hundreds to several kilos of voltage. With MOSFET's suitable for the application of class D audio amplifiers typically limited to the range of 200V - 800V, the semiconductor voltage stress becomes a key limitation for these applications.

Analysis:

The three fundamental configurations of the multilevel inverters are the flying capacitor, diode clamped and stacked H-brigdes. Figure 1 illustrates the three level version of each of these three configurations. Each configuration can be extended to higher levels if necessary. The flying capacitor configuration is advantageous, because of its low number of semiconductors, and the fact that it does not require isolated sources. Diodes are further more not a good choice for audio applications due to their nonlinear characteristic. Maintaining the charge balance of C_{Fly} is on the other hand a concern for the flying capacitor configuration. This task can be achieved though proper design of the control loop, which will be addressed later.



(a) Flying capacitor. (b) Diode clamped.



(c) Stacked H-brigdes.

Figure 1: Fundamental multilevel inverter configurations.

Ripple current:

The peak to peak inductor current ripple of the three level single ended multilevel inverter as shown in figure 1, is [18, 19]

$$\Delta i_{3L_{Pk-pk}} = \begin{cases} \frac{2V_S(0.5-D)D}{Lf_{Sw}} & for \quad D \leq 0.5 \\ \frac{2V_S(1-D)(D-0.5)}{Lf_{Sw}} & for \quad D > 0.5 \end{cases}$$

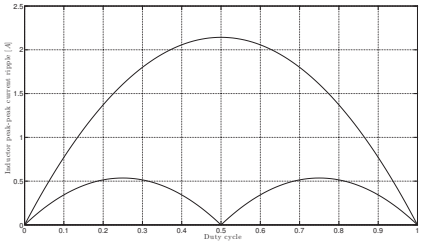


Figure 2: Indutctor current ripple.

The current ripple is plotted in figure 2 together with the ripple of the comparable synchronous buck converter. Two important observations are to be made. First, the ripple current is zero at 50 % of duty cycle, eliminating idle conduction losses. Second, the peak ripple is 4 times smaller than the comparable buck type solution.

The flying capacitor:

The flying capacitor should be selected large enough not to promise the THD. A small flying capacitor will cause pumping and thus increase THD. Sizing of the flying capacitor is investigated in Matlab/Simulink. The Simulink profile is given in figure 3. A control loop is included in the simulation. The purpose of the loop is to balance the flying capacitor and ensure damping of the output filter. A later section will address the control strategy.

The simulation operates at a step size of 10 ns with the solver of Euler. A load capacitor, C_{DEAP}, of 100 nF is used, and it is assumed, that $C_{DEAP} = C_{Fly}$. Figure 4 and 5 shows the simulated Fast Fourier Transform (FFT) spectrum for the reference frequency of 1 kHz. The output voltage and the voltage across C_{Fly} are plotted. Significant odd harmonics are observed in the voltage across C_{Fly}. Modulation indexes of 0.33 and 0.67 are considered. THD below 1 % is observed at the modulation of 0.67. The design parameters of the prototype amplifier are the ones used for the simulation, and will be presented in the Experimental Results section.

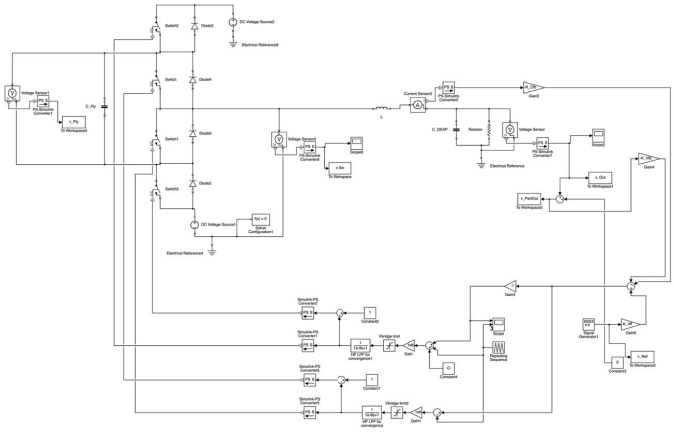
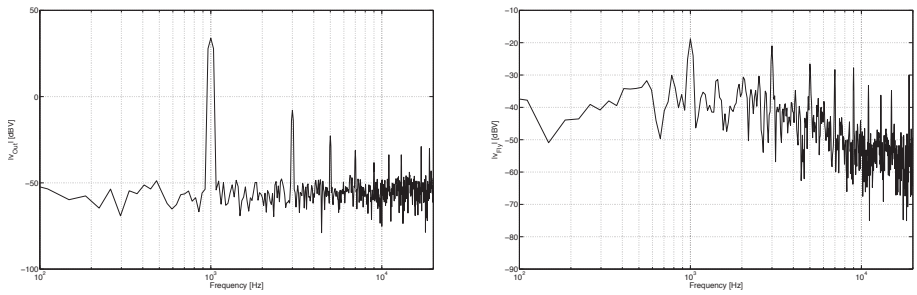


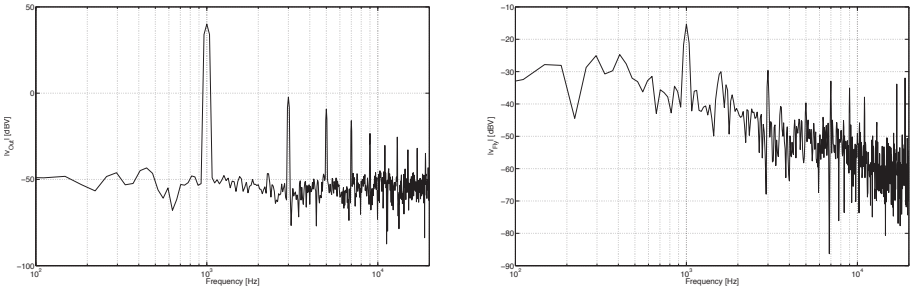
Figure 3: Simulink simulation profile using the Simscape toolbox.



(a) Output voltage.

(b) Flying capacitor voltage.

Figure 4: Simulated FFT spectrum for modulation index of 0.33.

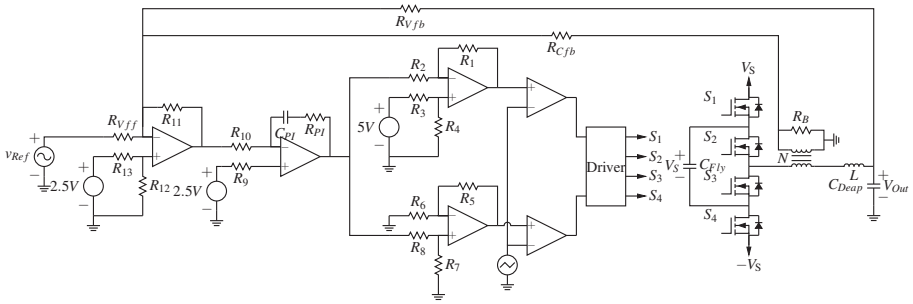


(a) Output voltage. (b) Flying capacitor voltage.

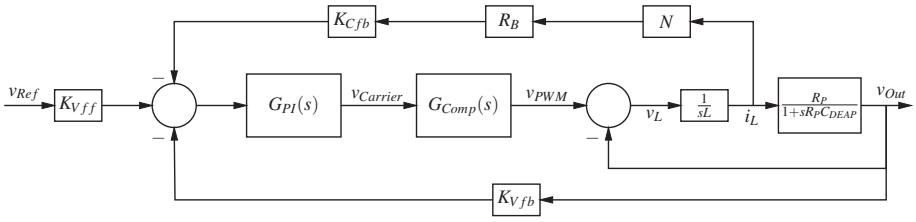
Figure 5: Simulated FFT spectrum for modulation index of 0.67.

Control:

When selecting a flying capacitor power stage, balancing the charge of C_{Fly} becomes a key concern. A number of publications have dealt with the issue of balancing the charge of the flying capacitor and lowering the voltage ripple with suitable modulations schemes [20, 21]. These publications assume the inductive and resistive load found in motor drive applications. An important concept is the flying capacitor self- or natural-balancing [22]. It is suggested in [22], that a capacitive load will not necessary ensure natural-balancing. Consequently is it proposed to implement force balancing. A very simple way of implementing active or forced balancing is proposed in [18] by control of the inductor current. This approach is particular suitable for the application of a capacitive load, as the current loop effectively balance the charge between C_{Fly} and C_{DEAP}. Figure 6 shows a schematic of the power stage with control. The inductor current is sensed through a current sense transformer. Low frequency loop gain is achieved by the addition of a voltage loop. A PI-controller is used under fixed frequency operation. Phase shifted error signals is utilised for generating the three level PWM signal. A small-signal model of the amplifier is given in figure 6(b). $G_{Comp}(s)$ is the combined small-signal transfer function of comparators and power stage. It is assumed, that C_{Fly} is large enough to be considered an ideal voltage source.



(a) Schematic with single-supply control circuitry.



(b) Small-signal model.

Figure 6: Flying capacitor class D amplifier with control.

Design:

Using the definitions of figure 6(b), the open loop gain of the current loop is

$$Tf_{Ol_{Cm}}(s) = K_{Cfb}R_B N G_{PI}(s)G_{Comp}(s)\frac{C_{DEAP}s+\frac{1}{R_P}}{s^2LC_{DEAP}+s\frac{L}{R_P}+1} \quad (1)$$

while the closed loop

$$Tf_{Cl_{Cm}}(s) = \frac{G_{PI}(s)G_{Comp}(s)\left(C_{DEAP}s+\frac{1}{R_P}\right)}{s^2LC_{DEAP}+s\frac{L}{R_P}+1+G_{PI}(s)G_{Comp}(s)K_{Cfb}NR_N\left(C_{DEAP}s+\frac{1}{R_P}\right)} \quad (2)$$

The complete open loop gain of the combined current and voltage loop is

$$Tf_{Ol_{Vm}}(s) = Tf_{Cl_{Cm}}(s)K_{Vfb}\frac{R_P}{sR_PC_{DEAP}+1} \quad (3)$$

while the closed loop

$$Tf_{Cl_{Vm}}(s) = \frac{Tf_{Cl_{Cm}}(s)R_P}{RC_{DEAP}s+1+Tf_{Cl_{Cm}}(s)R_P} \quad (4)$$

The control coefficients are defined as

$$K_{Vfb} = \frac{R_{Vff}||R_{Cfb}}{R_{Vff}||R_{Cfb}+R_{Vfb}} \quad (5)$$

$$K_{Cfb} = \frac{R_{Vfb}||R_{Vff}}{R_{Vfb}||R_{Vff}+R_{Cfb}} \quad (6)$$

$$K_{Vff} = \frac{R_{Vfb}||R_{Cfb}}{R_{Vfb}||R_{Cfb}+R_{Vff}} \quad (7)$$

Experimental results:

A $\pm$ 300 V flying capacitor multilevel inverter based class D amplifier driving a 100 nF load in the midrange region of 0.1-3.5 kHz is used for experimental verification. Figure 7 shows the prototype amplifier, which is based around two Si8235 isolated gate drivers and SPA08N80C3 MOSFET's. The control scheme is implemented using a single-supply control circuitry with THS4221 operational amplifiers and LMV7219 comparators. Current measurement is performed using the current sense transformer, CST1-070LB, from Coilcraft. NOR-gates (SN74AHC1G02DBVR) and RC-circuits generates the required deadtime. A polypropylene capacitor is used as dummy load to perform all measurements. Table I and II shows the key component and design values of the prototype amplifier. Time domain waveforms are shown in figure 8(a) for the reference frequency of 1 kHz and a modulation index of 0.67.

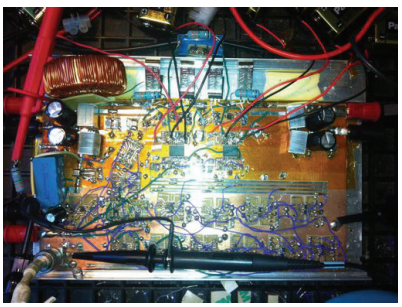


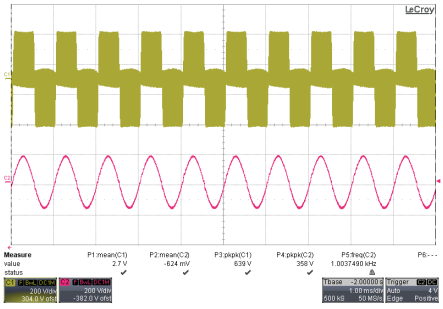
Figure 7: Prototype amplifier.

	Designator	Value
Switching frequency	f_{Sw}	167 kHz
Output filter inductance	L	200 uH
DEAP Capacitance	C_{DEAP}	100 nF
Flying Capacitance	C_{Fly}	100 nF
Supply voltage	$\pm V_S$	$\pm 300V$
Closed loop gain	A_V	150 $\frac{V}{V}$

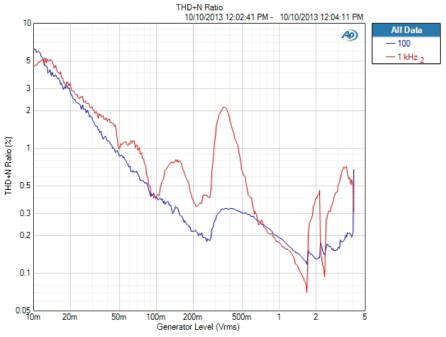
Table I: Design parameters.

Table II: Component values

Component	Value
R_B	100 Ω
C_{PI}	10 nF
R_{PI}	1 $k\Omega$
R_{Cbf}	2 $k\Omega$
R_{Vff}	2 $k\Omega$
R_{Vfb}	300 $k\Omega$
R_1, R_2, R_3, R_4, R_5, R_6, R_7, R_8, R_9, R_{10}, R_{11}, R_{12} and R_{13}	1 $k\Omega$
N	$\sqrt{\frac{200nH}{3000uH}} \approx 0.008$



(a) Time domain waveforms with a reference frequency of 1 kHz and modulation index of 0.67. The switching node voltage is the top trace, while the output voltage is the bottom trace.



(b) THD+N of the prototype for the reference frequencies of 100 Hz and 1 kHz.

Figure 8: Measuring results.

THD+N and closed-loop response

THD+N is measured using an APX525 audio analyzer and a voltage attenuation interface. The voltage attenuation interface is necessary in order to protect the input-stage of the audio analyzer. Design and implementation of the voltage attenuation interface is well-described in the literature [7, 23]. Figure 8(b) gives the measured THD+N as a function of the reference voltage for the frequencies of 100 Hz and 1 kHz. THD+N is below 1% over a significant part of the operation range. Noise is the dominating factor at low reference voltages. As the signal-to-noise ratio improves THD+N drops linearly to a reference voltage of around 200 mV. In the region of v_{Ref} = 200–500 mV the dead-time distortion becomes the dominating source of none-linearity. At high reference voltages (above 1 V) total harmonic distortion is observed before clipping.

Conclusion:

The concept of multilevel inverters as power stages in class D audio amplifiers is introduced. It is proposed to drive capacitive transducers from a three-level modulated flying capacitor class D amplifier. Experimental verification is conducted on a ± 300 V prototype amplifier driving a 100 nF load in the midrange region of 0.1-3.5 kHz. THD+N below 1 % is reported over a significant part of the operation range.

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Dennis Nielsen, Arnold Knott and Michael A.E. Andersen, "Class D audio amplifier with 4th order output filter and self-oscillating full-state hysteresis based feedback driving capacitive transducers", 16th Conference on Power Electronics and Applications, EPE14-ECCE Europe, Lappeenranta, Finland.

Class D audio amplifier with 4th order output filter and self-oscillating full-state hysteresis based feedback driving capacitive transducers

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Keywords

Sliding mode control, High voltage power converters, Drive, Active damping, Amplifiers

Abstract

A practical solution is presented for the design of a non-isolated high voltage DC/AC power converter. The converter is intended to be used as a class D audio amplifier for a Dielectric Electro Active Polymer (DEAP) transducer. A simple and effective hysteretic control scheme for the converter (buck with fourth-order output filter) is developed and analyzed. The proposed design is verified experimentally by a 125 VAR prototype amplifier, capable of delivering a peak output voltage of 240 V within the frequency range of 100 Hz – 3.5 kHz. A peak efficiency of 87 % is reported.

Introduction:

Sound reproduction systems are commonly build around class D audio amplifiers due to their superior cost, size and efficiency compared to their linear counterparts [1, 2, 3, 4, 5]. While these audio systems are dominating the market of sound reproduction, they still suffer from the poor efficiency imposed by the electrodynamic transducer. An alternative to the electrodynamic transducer is the capacitive transducer. Capacitive transducers are most known from their usage in electrostatic loudspeakers, however Dielectric Electro Active Polymers (DEAP) can also be used to form a capacitive transducer [6, 7, 8]. With the goal of creating smaller, cheaper and more efficient audio systems it is proposed to use a class D amplifier as driver of the capacitive transducer [9, 10]. Class D amplifiers driving a capacitive transducer without the use of audio or high frequency linked transformers, is an area of research with little to no publications. This paper addresses the issue of limited frequency response and high series resistance of capacitive transducers. The focus of the paper is placed upon Dielectric Electro Active Polymer (DEAP) transducers, however the concept can easily be extended to other capacitive transducers like piezoelectric ones.

A push DEAP transducer is shown in figure 1, while the measured impedance of the transducer is presented in figure 2. It is observed from figure 2, that the transducer cannot be expected to act as a capacitor for frequencies above 100 kHz. This limits the switching frequency significantly, if the output filter is constructed entirely by an inductor and the DEAP. Film or ceramic capacitors could be placed in parallel with the DEAP transducer. This will improve the frequency response. However it will also increase the reactive output power of the amplifier, because the capacitive load is increased. Another concern of the DEAP transducer is the series resistance. Older versions of the DEAP material [6] exhibited series resistance up to 50 Ω, while the present versions are specified within the region of 1–10 Ω. The connection between the DEAP transducer and the surrounding electronics is even more complicated than that of the film capacitor. DEAP transducers are constructed by printing compliant electrodes on a silicone membrane. The contact is performed on a surface exposed to significant mechanical stress.

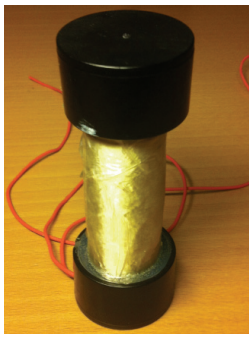
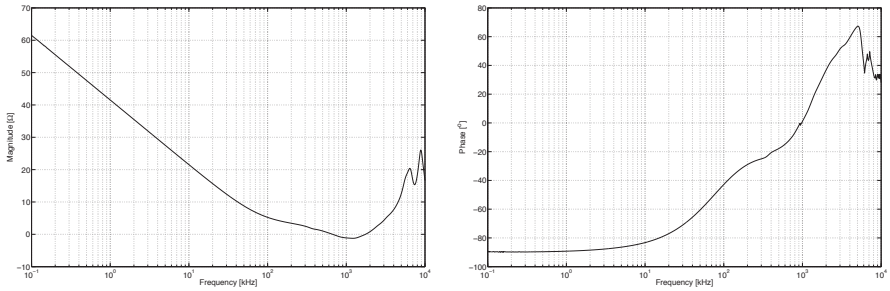


Figure 1: DEAP push transducer.



(a) Magnitude. (b) Phase.

Figure 2: Measured impedance.

Theory

Due to the high series resistance of the DEAP transducer, the magnitude of the ripple current becomes a concern. Conduction losses will dominate, if the ripple current becomes to high. This is both a problem in terms of efficiency, but also because of the reduced lifetime of the contact interface. In order to estimate the switching frequency required for maintaining sufficiently low current ripple with second-order and fourth-order output filtering, respectively, consider the Fourier series representing of a pulse-width modulation signal (D = 0.5)

$$v_{PWM}(t) = \frac{4V_S}{\pi} sin(2\pi ft) + \frac{4V_S}{3\pi} sin(3 \cdot 2\pi ft) \tag{1}$$

$$\frac{4V_S}{5\pi} sin(5 \cdot 2\pi ft) + ... \tag{2}$$

Using fundamental component analysis it can be assumed that

$$v_{PWM}(t) \approx \frac{4V_S}{\pi} sin(2\pi ft) \tag{3}$$

The transfer function from input voltage to capacitor current for the second-order output filter is

$$\frac{i_C(s)}{v_{PWM}(s)} = \frac{C_{DEAP}s}{C_{DEAP}L_1 s^2 + \frac{L}{R}s + 1} \tag{4}$$

If a signal frequency is applied well above $\omega_0 = \frac{1}{\sqrt{L_1 C_{DEAP}}}$, equation (4) can be simplified to

$$\left| \frac{i_C(j\omega)}{v_{PWM}(j\omega)} \right|_{\omega \gg \omega_0} \cong \frac{1}{L_1 \omega} \tag{5}$$

The current ripple is found by multipling equation (3) with equation (8)

$$\Delta i_C = \frac{2V_S}{\pi^2 Lf} \tag{6}$$

For the fourth-order output filter a similar approach can show that

$$\frac{i_C(s)}{v_{PWM}(s)} = \frac{C_{DEAP}s}{s^4 L_1 L_2 C_1 C_{DEAP} + s^3 \frac{L_1 L_2 C_1}{R} + s^2(L_1 C_{DEAP} + L_1 C_1 + L_2 C_{DEAP}) + s\frac{L_1+L_2}{R} + 1} \tag{7}$$

$$\left| \frac{i_C(j\omega)}{v_{PWM}(j\omega)} \right|_{\omega \gg \omega_0} \cong \frac{1}{L_1 L_2 C_1 \omega^3} \tag{8}$$

$$\Delta i_C = \frac{V_S}{2L_1 L_2 C_2 \pi^4 f^3} \tag{9}$$

Consider a case study where $V_S = 300$ V, $L_1 = 200\mu H$ and $f_{Sw} = 285$ kHz, the current ripple through the DEAP transducer becomes $\Delta i_C = \frac{2 \cdot 300V}{200\mu H 2\pi 285kHz} = 1.59$ A peak for the 2th order output filter solution. Assuming $L_1 = L_2 = 200\mu H$ and $C_1 = 100nF$, $\Delta i_C = \frac{300V}{2 \cdot 200\mu H 200\mu H 100nF \pi^4 (285kHz)^3} = 16.6$ mA peak for the 4th order output filter solution. With a worst case series resistance of 10 Ω, the 2th order output filter solution will yield a loss of 8.43 W, while the loss of the 4th order output filter solution is 0.92 mW. For an amplifier producing a maximum output power of 125 Var, the 4th order output filter solution becomes the right choice in terms of efficiency. A formal definition of the efficiency will be given later. Another benefit of the 4th order output filter solution is the possibility for a film capacitor to be used in the first LC-filter stage. The high frequency content will then flow through a capacitor with a frequency response much better than that of the DEAP transducer.

Control

Hysteresis based self-oscillating control schemes have received great interest in class D audio amplifiers due to the superior loop gain [11, 12, 13]. The switching frequency is defined as

$$f_{Sw}(D) = \frac{D(1-D)}{2\frac{V_{Hyst}}{K} + t_D} \tag{10}$$

With D been the duty cycle, t_D the control-loop delay, v_{Hyst} the height of the hysteresis window, and

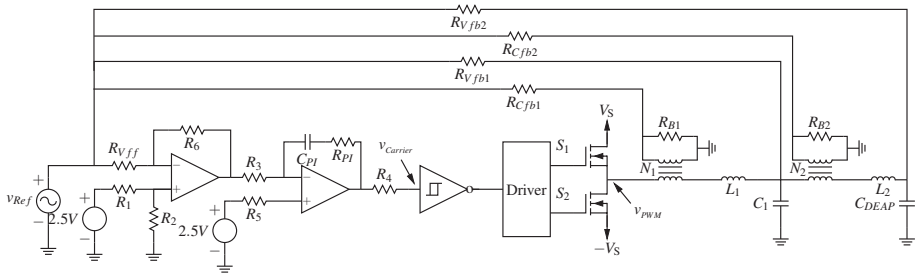
$$K = 2V_S \times step\{\lim_{s \to \infty} G_{Ctrl}(s)\} \tag{11}$$

For the purpose of designing the self-oscillation control-loop, the controller transfer function must be defined as

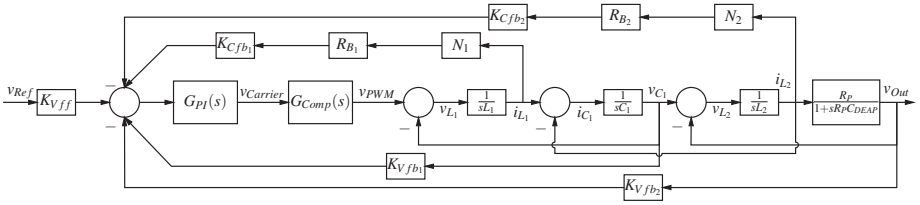
$$G_{Ctrl}(s) = \frac{v_{Carrier}(s)}{v_{PWM}(s)} \tag{12}$$

$$= K_{Vfb_1}\frac{v_{C_1}(s)}{v_{PWM}(s)} + K_{Vfb_2}\frac{v_{Out}(s)}{v_{PWM}(s)} + K_{Cfb_1}\frac{i_{L_1}(s)}{v_{PWM}(s)} + K_{Cfb_2}\frac{i_{L_2}(s)}{v_{PWM}(s)} \tag{13}$$

where definitions from figure 3(a) is utilized.



(a) Schematic with single-supply control circuitry.



(b) Small-signal model.

Figure 3: Prototype class D amplifier with 4th order output filter and control.

Transfer functions

The transfer functions of equation (13) are defined as

$$\frac{v_{Out}(s)}{v_{PWM}(s)} = \frac{1}{s^4L_1L_2C_1C_2 + s^3\frac{L_2L_1C_1}{R_P} + s^2(C_1L_1 + L_2C_2 + L_1C_2) + s\frac{L1+L2}{R_P} + 1} \tag{14}$$

$$\frac{v_{C_1}(s)}{v_{PWM}(s)} = \frac{s^2L_2C_2 + s\frac{L_2}{R_P} + 1}{s^4L_1L_2C_1C_2 + s^3\frac{L_2L_1C_1}{R_P} + s^2(C_1L_1 + L_2C_2 + L_1C_2) + s\frac{L1+L2}{R_P} + 1} \tag{15}$$

$$\frac{i_{L_1}(s)}{v_{PWM}(s)} = \frac{s^4L_1L_2C_1C_2 + s^3\frac{L_2L_1C_1}{R_P} + s^2(C_1L_1 + L_1C_2) + s\frac{L1}{R_P}}{sL_1(s^4L_1L_2C_1C_2 + s^3\frac{L_2L_1C_1}{R_P} + s^2(C_1L_1 + L_2C_2 + L_1C_2) + s\frac{L1+L2}{R_P} + 1)} \tag{16}$$

$$\frac{i_{L_2}(s)}{v_{PWM}(s)} = \frac{s^2L_2C_2 + s\frac{L_2}{R_P}}{sL_2(s^4L_1L_2C_1C_2 + s^3\frac{L_2L_1C_1}{R_P} + s^2(C_1L_1 + L_2C_2 + L_1C_2) + s\frac{L1+L2}{R_P} + 1)} \tag{17}$$

The feedback coefficients defined in figure 3(b) are

$$K_{Vfb_1} = \frac{R_{Vfb2}||R_{Cfb1}||R_{Cfb2}||R_{Vff}}{R_{Vfb2}||R_{Cfb1}||R_{Cfb2}||R_{Vff} + R_{Vfb1}} \tag{18}$$

$$K_{Vfb_2} = \frac{R_{Vfb2}||R_{Cfb1}||R_{Cfb2}||R_{Vff}}{R_{Vfb2}||R_{Cfb1}||R_{Cfb2}||R_{Vff} + R_{Vfb2}} \tag{19}$$

$$K_{Cfb_1} = \frac{R_{Vfb2}||R_{Cfb1}||R_{Cfb2}||R_{Vff}}{R_{Vfb2}||R_{Cfb1}||R_{Cfb2}||R_{Vff} + R_{Cfb1}} \tag{20}$$

$$K_{Cfb_2} = \frac{R_{Vfb2}||R_{Cfb1}||R_{Cfb2}||R_{Vff}}{R_{Vfb2}||R_{Cfb1}||R_{Cfb2}||R_{Vff}+R_{Cfb2}} \quad (21)$$

$$K_{Vff} = \frac{R_{Vfb2}||R_{Cfb1}||R_{Cfb2}||R_{Vff}}{R_{Vfb2}||R_{Cfb1}||R_{Cfb2}||R_{Vff}+R_{Vff}} \quad (22)$$

Design

Using equation (13) and equation (11), the constant K can be derived

$$K = \frac{2V_s K_{Cfb_1} N_1 R_{B_1}}{L_1} \quad (23)$$

It is assumed, that the inner current loop is dominating at the high frequencies.

Experimental results:

A $\pm$ 300 V half-bridge based class D amplifier driving a 100 nF load in the midrange region of 0.1-3.5 kHz is used for experimental verification. The amplifier is build around a Si8235 isolated gate driver and SPA08N80C3 MOSFET's. Figure 4(a) shows a picture of the prototype amplifier. Design parameters are presented in Table I, while derived component values are gathered in Table II.

Efficiency

When driving a DEAP transducer it is appropriate to give a formal definition of the term efficiency. The first order approximation will yield a capacitive load. Accordingly no real power will be delivered to the load. Efficiency will thus be defined as

$$\eta = \frac{P_{Out}}{P_{Out}+P_{In}} \quad (24)$$

where $P_{Out} = \frac{V_{rms}^2}{\left(\frac{1}{2\pi f_{Ref} C_{Deap}}\right)}$, is the reactive power delivered to the load, and P_{In} corresponds to the real power consumed by the amplifier. This definition of the term efficiency will be used throughout the paper.

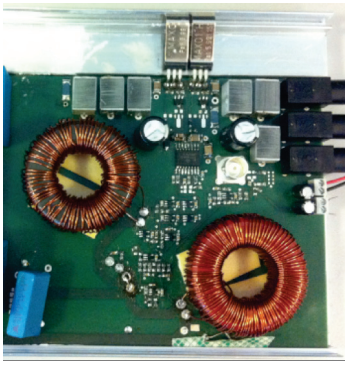
The measured efficiency can be seen in figure 4(b). The efficiency is defined in accordance with equation 24. Note, that the efficiency at 100 Hz is below 40 %. Because the output voltage is kept fixed with respect to frequency, the reactive output power will drop inversely proportional with the frequency. At 100 Hz the switching loss becomes comparable with the reactive output power. An efficiency above 80 % is achieved for the frequencies of 1 and 3.5 kHz. Voltage mode control of electrostatic transducers is preferred for applications where displacement is of concern. Charge mode control ensures greater linearity at the expense of displacement [14].

	Designator	Value
Idle switching frequency	f_{Sw}	285 kHz
Output filter inductance	L_1	200 uH
Output filter inductance	L_2	200 uH
Output filter capacitance	C_1	100 nF
DEAP Capacitance	C_{DEAP}	100 nF
Supply voltage	$\pm V_S$	$\pm 300V$
Closed loop gain	A_V	75 $\frac{V}{V}$

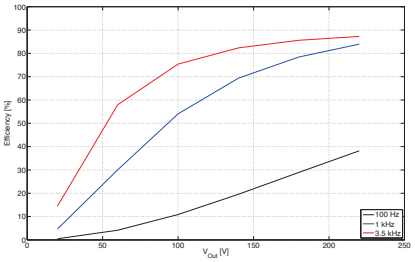
Table I: Design parameters.

Component	Value
R_{B_1}	110 Ω
R_{B_2}	10 Ω
C_{PI}	1.5 nF
R_{PI}	1 $k\Omega$
R_{Cbf_1}	4 $k\Omega$
R_{Cbf_2}	4 $k\Omega$
R_{Vff}	2 $k\Omega$
R_{Vfb_1}	300 $k\Omega$
R_{Vfb_2}	300 $k\Omega$
R_1, R_2, R_3, R_4, R_5 and R_6	1 $k\Omega$
N_1 and N_2	$\sqrt{\frac{200nH}{980uH}} \approx 0.014$

Table II: Component values.



(a) Picture of prototype amplifier.



(b) Efficiency.

Figure 4: Prototype amplifier.

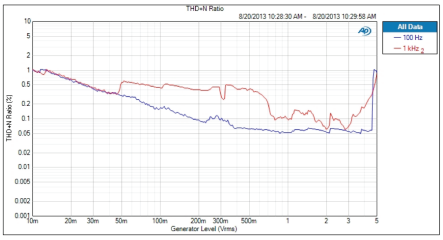


Figure 5: THD+N of the prototype for reference frequencies of 100 Hz and 1 kHz.

THD+N

THD+N is measured using an APX525 audio analyzer and a voltage attenuation interface. The voltage attenuation interface is necessary in order to protect the input-stage of the audio analyzer. Design and implementation of the voltage attenuation interface is well-described in the literature [10, 15]. Figure 5 gives the measured THD+N as a function of the reference voltage for the frequencies of 100 Hz and 1 kHz. THD+N is below 0.1% over a significant part of the operation range for the reference frequency of 100 Hz. Noise is the dominating factor in the measured THD+N.

Conclusion:

A class D audio amplifier with 4th order output filter for capacitive transducers is proposed and analyzed. The amplifier addresses the issues of high series resistance and limited frequency response of the capacitive transducers, potentially paving the way for increased industry adoption of this highly promising technology. THD+N below 0.1% is reported for the $\pm$ 300 V prototype amplifier producing a maximum of 125 Var at a peak efficiency of 87 %.

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Dennis Nielsen, Arnold Knott and Michael A. E. Andersen, "A Direct Driver for Electrostatic Transducers", 137 AES Convention, LA, USA

Audio Engineering Society

Convention Paper

Presented at the 137th Convention
2014 October 9–12 Los Angeles, USA

A Direct Driver for Electrostatic Transducers

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ABSTRACT

Electrostatic transducers represent a very interesting alternative to the traditional inefficient electrodynamic transducers. In order to establish the full potential of these transducers, power amplifiers which fulfill the strict requirements imposed by such loads (high impedance, frequency depended, nonlinear and high bias voltage for linearization) must be developed. This paper analyzes a power stage suitable for driving an electrostatic transducer under biasing. Measurement results of a $\pm$ 400 V prototype amplifier are shown. THD below 1% is reported.

INTRODUCTION:

Class D audio amplifiers are commonly used in sound reproduction systems due to their superior cost, size and efficiency compared to their linear counterparts [1, 2]. While these audio systems are dominating the market of sound reproduction, they still suffer from the poor efficiency imposed by the electrodynamic transducer. An alternative to the electrodynamic transducer is the capacitive transducer. Capacitive transducers are most known from their usage in electrostatic loudspeakers, however Dielectric Electro Active Polymers (DEAP) and piezoelectric ceramics can also be used to form a capacitive transducer [3, 4, 5]. With the goal of creating smaller, cheaper and more efficient audio systems it is proposed to use a class D amplifier as driver of the capacitive transducer [6, 7]. Class D amplifiers driving a capacitive transducer without the use of audio or high frequency linked transformers, is an area of research with little to no publications. This paper analyses a power stage suitable for driving a captive transducer under biasing.

THEORY:

Class D audio amplifiers driving the resistive and inductive load of the electrodynamic transducer are implemented using the half- and full-bridge power stages as shown in figure 1 and 2. These power stages does not provide the DC-biasing voltage required by capacitive transducers. The half-bridge power stage can be modified to allow for DC-operation by using a single supply implementation as shown in figure 3. Notice that the load now is assumed to be a purely capacitive load. The configuration achieves a sinusoidal waveform with a peak amplitude of $\frac{V_{CC}}{2}$ at the duty cycle of 0.5, corresponding to a DC-biasing voltage of $\frac{V_{CC}}{2}$. If a higher biasing is targeted, it will be at the cost of reduced peak amplitude.

In order not to loss peak amplitude with DC-biasing the

differential coupled class D power stage as shown in figure 4 is proposed. This configuration allows for operation at a DC-biasing voltage of V_{CC}, while maintaining the peak amplitude of $\frac{V_{CC}}{2}$.

The semiconductor voltage stress is also a key concern as capacitive transducers typically requires voltages of some hundreds to several kilos. Notice that the voltage stress across the Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) is identically in figure 3 and 4. An inconvenient consequence of the differential coupled class D power stage is the cost of two extra MOSFETs and an output filter, when comparing with figure 3.

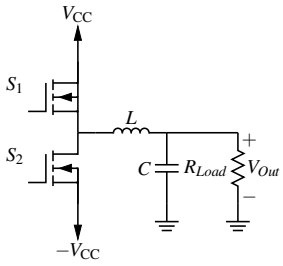


Figure 1: *Traditional half-bridge class D power stage.*

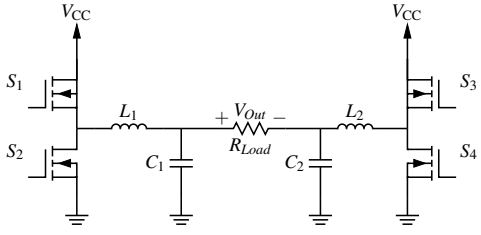


Figure 2: *Traditional full-bridge class D power stage.*

CONTROL:

The differential coupled class D power stage is constructed from two single suppled half-bridge power stages. Each half-bridge power stage has its own control scheme. A hysteresis based self-oscillating bandpass current mode control (BPCM) scheme is proposed in [8, 6] as an efficient way of implementing active damping of the second order output filter resonance, while ensuring high loop-gain. Implementation of the BPCM scheme is achieved by

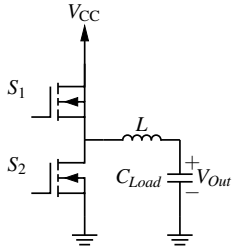


Figure 3: *Single supply half-bridge class D power stage.*

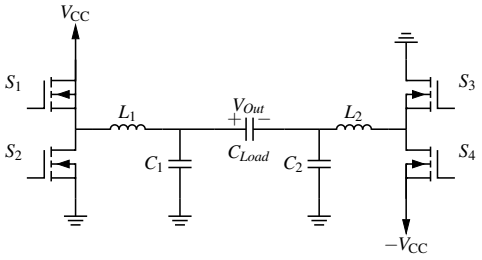


Figure 4: *Differential coupled class D power stage.*

sensing the inductor current through a current sense transformer. A simple voltage divider allows for the output voltage to be included in the control loop. Implementation of a single half-bridge power stage with control circuity is shown in figure 6 together with the small signal model.

A conceptual diagram of the complete differential coupled class D power stage is shown in figure 5. The half-bridges is operated at a 180^o phase shift, and a synchronisation circuit ensures that aliasing does not occur.

Self-oscillation

Oscillation is ensured by shaping the open-loop frequency response to have a phase shift of 360^o and unity gain at the targeted switching frequency. This is the Barkhausen Oscillation criterium. It can be shown, that the switching frequency is described by the function [9, 10]

$$f_{Sw}(D) = \frac{D(1-D)}{2\frac{V_{Hyst}}{K} + t_D} \tag{1}$$

With K defined as:

$$K = V_{CC} \times step\{\lim_{s\to\infty} G_{Ctrl}(s)\} \tag{2}$$

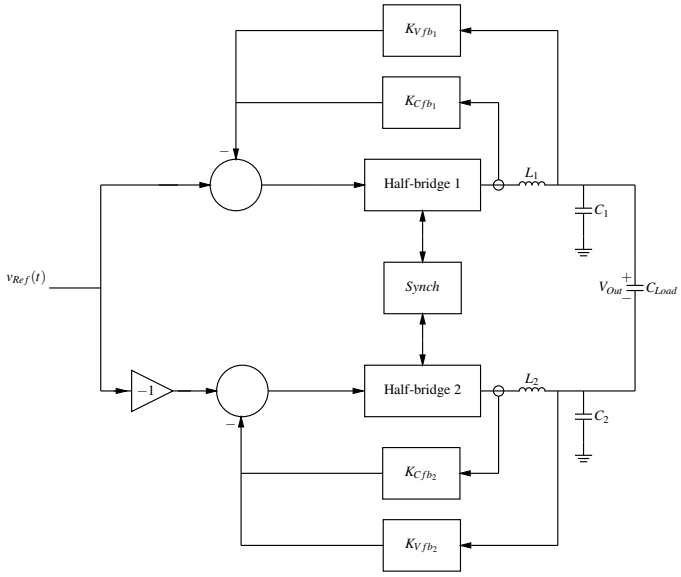


Figure 5: *Conceptual diagram of the complete differential coupled class D power stage.*

For the purpose of designing the self-oscilation control loop, the controller transfer function must be defined

$$G_{Ctrl}(s) = \frac{v_{Carrier}(s)}{v_{PWM}(s)} \quad (3)$$

$$= G_{PI}(s)\left(K_{Vfb} + K_{Cfb}R_{Sense}NCs\right)\frac{1}{LCs^2+1} \quad (4)$$

K can be derived using equation (2) and (4)

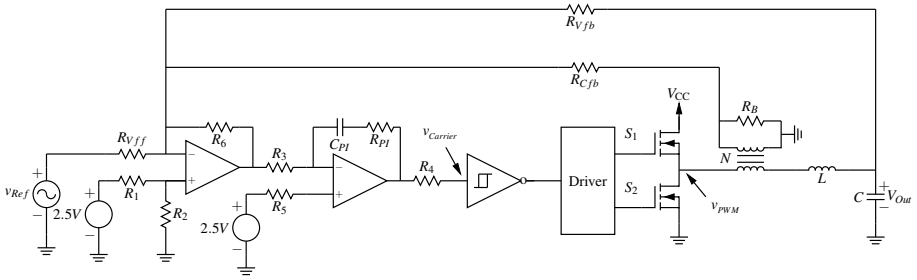
$$K = \frac{V_{CC}K_{Cfb}NR_{Sense}}{L} \quad (5)$$

Synchronisation:
Synchronisation of multiple carriers is a known issue in three level modulated full-brigde class D amplifiers. This paper utilizes the fact, that self-oscillating systems have a inherent tendency of locking to external frequencies. As proposed in [2] a simple high impedance path between two oscillators, will cause these to synchronise. Figure 7 shows how two carries can be synchronised using coupled hysteresis windows. Implemention is preformed with single supple comparators.

Table 1: *Component values*

Component	Value
R_B	100 Ω
C_{PI}	10 nF
R_{PI}	1 $k\Omega$
R_{Cbf}	2 $k\Omega$
R_{Vff}	2 $k\Omega$
R_{Vfb}	300 $k\Omega$
R_1, R_2, R_3, R_4, R_5 and R_6	1 $k\Omega$
N	$\sqrt{\frac{200nH}{980uH}} \approx 0.014$
R_{H2}, R_{H3}, R_{H6} and R_{H7}	10 $k\Omega$
R_{C1} and R_{C2}	1 $k\Omega$
R_{H1} and R_{H5}	15 $k\Omega$
R_{H4}	100 $k\Omega$

EXPERIMENTAL RESULTS:
A ± 400 V class D amplifier driving a 100 nF load in the midrange region of 100 Hz – 3.5 kHz is used for experimental verification. The amplifier is build around two Si8235 isolated gate driver and STW25N95K3 MOSFET's. Figure 8 shows a picture of the prototype amplifier. Component values are collected in table 1.



(a) Schematic with single-supply control circuitry.

(b) Small-signal model.

Figure 6: *Class D amplifier with BPCM control.*

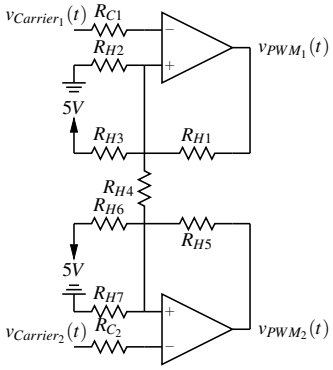


Figure 7: *Synchronisation of multiple carriers.*

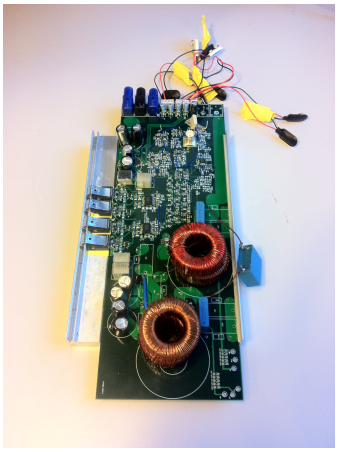


Figure 8: *Prototype amplfier.*

Figure 9 shows the differential switching node and output voltages, when operating with a reference frequency of 100 Hz and output voltage of 250 V_{pkpk}. The DC-biasing voltage is 400 V corresponding to a duty cycle of 0.5. An idle switching frequency of 84 kHz is observed, close to the targeting 85 kHz of table 2.

Table 2: *Design parameters*

	Designator	Value
Idle switching frequency	f_{Sw}	85 kHz
Output filter inductance	L_1 and L_2	300 uH
Load capacitance	C_{Load}	100 nF
Supply voltage	$\pm V_{CC}$	$\pm$ 400 V
Filter capacitance	C_1 and C_2	100 nF
Closed loop voltage gain		48 dB

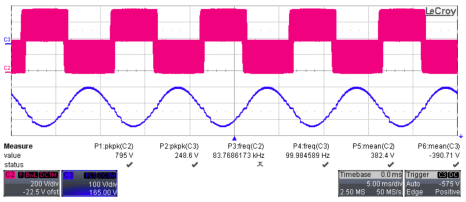


Figure 9: *Waveforms of prototype amplifier.*

THD+N

THD+N is measured using an APX525 audio analyzer and a differential probe (1/200). Figure 10 gives the measured THD+N as function of the reference voltage for the frequencies of 100 Hz and 1 kHz. THD+N is below 1% over a significant part of the operation range for the reference frequency of 100 Hz. All measurements are performed using a 4 kHz low pass. This is valid as a midrange application is considered.

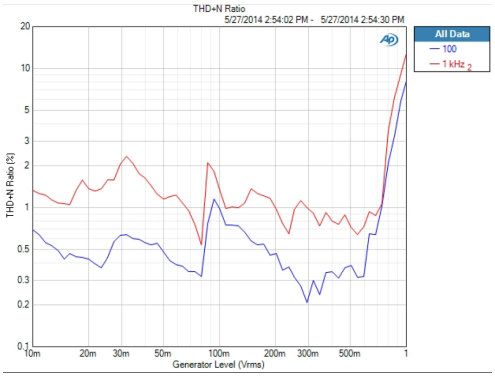


Figure 10: *THD+N (100 Hz and 1 kHz).*

CONCLUSION:

A class D audio amplifier with differential coupled and phase shifted half-bridge power stages is proposed and analyzed. The amplifier addresses the issue of driving a capacitive transducer under biasing. THD+N below 1% is reported for the $\pm$ 400 V prototype amplifier producing a maximum of 225 Var into a 100 nF capacitive load. The design of the amplifier is targeting the midrange region of the audio bandwidth (100 Hz – 3.5 kHz).

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Dennis Nielsen, Arnold Knott and Michael A. E. Andersen, "Comparative Study of Si and SiC MOSFETs for High Voltage Class D Audio Amplifiers", 137 AES Convention, LA, USA.

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Presented at the 137th Convention
2014 October 9–12 Los Angeles, USA

Comparative Study of Si and SiC MOSFETs for High Voltage Class D Audio Amplifiers

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ABSTRACT

Silicon (Si) Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) are traditional utilised in class D audio amplifiers. It has been proposed to replace the traditional inefficient electrodynamic transducer with the electrostatic transducer. This imposes new high voltage requirements on the MOSFETs of class D amplifiers, and significantly reduces the selection of suitable MOSFETs. As a consequence it is investigated, if Silicon-Carbide (SiC) MOSFETs could represent a valid alternative. The theory of pulse timing errors are revisited for the application of high voltage and capactive loaded class D amplifiers. It is shown, that SiC MOSFETs can compete with Si MSOFETs in terms of THD. Validation is done using simulations and a $\pm$ 500 V amplifier driving a 100 nF load. THD+N below 0.3 % is reported.

INTRODUCTION:

Class D amplifiers are widely used due to their high efficiency. It is well-known, that the system efficiency of a complete audio system, amplifier and loudspeaker, is limited by the poor efficiency of the electrodynamic transducer. Consequently, electrostatic transducers are investigated as an valid alternative. Electrostatic loudspeakers are most known for their usage in electrostatic loudspeakers, however Dielectric Electro Active Polymers (DEAP) and piezoelectric ceramic can also be used to form a electrostatic or capacitive transducer. The high voltage requirements of the capacitive transducer imposes a new challenge, when selecting MOSFETs for the class D amplifier. This paper revisits the theory of pulse timing errors for capacitive loaded class D amplifiers, and performs a comparative study of high voltage Si and SiC MOSFET suitable for the application of audio [1].

THEORY:

This paper will be limited to the half-bridge class D power stage of figure 1. The theory can however be extended to full-bridge configurations. Several publications have

analyzed the influence of pulse-timing errors on THD [2, 3, 4, 5]. These are traditional divided into the categories:

- Dead-time distortion.
- Finite switching speed.
- Conduction state errors.

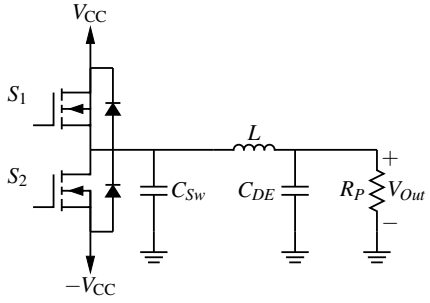


Figure 1: *Half-Bridge class D amplifier.*

Class D amplifiers driving the resistive and inductive load of an electrodynamic transducer is typically operated at hard switching. This is done in order to reduce dead-time distortion. High voltage class D amplifiers for capacitive transducers relies on soft-switching or Zero Voltage Switching (ZVS) of the MOSFETs for achieving high efficiency and low noise-floor [6, 7].

MODELLING:

When operating the power stage at ZVS, the dead-time distortion becomes a key concern. It is shown in [4], that dead-time distortion is a function of the ratio between reference and ripple current. This section analyzes dead-time distortion for a class D amplifier driving a capacitive load. Voltage mode control is assumed, meaning that the output current no longer can be considered constant with respect to frequency. This is unlike the case of driving an electrodynamic loudspeaker, where the load typically is assumed being resistive, and those the output current does not change with frequency. Let the THD arising from dead-time distortion being defined as [4]

$$THD_d(M,\alpha_d,\alpha_I) = \frac{\Delta(\alpha_I)\sqrt{\sum_{i=2}^{N_{Max}}\left[2\alpha_d\frac{sin(i\frac{\pi}{2})}{i\frac{\pi}{2}}\right]^2}}{M-\alpha_d\frac{4}{\pi}\Delta(\alpha_I)}$$

where the dead-time delay factor is the ratio of the dead-time to the period of the switching frequency

$$\alpha_d = \frac{t_{Dead}}{T_{sw}} \tag{1}$$

and the ripple current factor

$$\alpha_I = \frac{\Delta i_L(M)}{i_{Ref}(M)} \tag{2}$$

The ripple current factor is the amplitude of the ripple current divided by the reference current. Both being functions of the modulation index, M.

Using the ripple current factor of equation 2, it is defined that

$$\Delta(\alpha_I) = \begin{cases} 0 & i_{Ref}(M) \leq \Delta i_L(M) \\ \frac{\frac{\pi}{2}-arcsin(\alpha_I)}{\frac{\pi}{2}} & i_{Ref}(M) > \Delta i_L(M) \end{cases} \tag{3}$$

Similar results can be found in [8].

The ripple current of the half-bridge power stage in figure 1 can be defined as

$$\Delta i_L = 2V_{CC}\frac{D-D^2}{Lf_{Sw}} \tag{4}$$

Transformation between modulation index and duty cycle is performed using the relation $D(t) = \frac{1}{2}(Msin(2\pi f_{Ref}t)+1)$.

For most practical applications $i_{Ref}(M) \leq \Delta i_L(M)$, as the high impedance of a capacitance transducer calls for small currents. Equation 1 thus predict zero dead-distortion, and the question arises as to, what the dominating source of distortion is. The answer is, that equation 1 does not take into account the trapezoidal waveform of the switching node voltage during ZVS.

ZVS

ZVS is ensured by allowing the inductor current to charge and discharge the equivalent switching node capacitance, C_{Sw}, before performing a switching transition. Assuming that the dead-time required to achieve ZVS is significant smaller that the switching period, the inductor current can be considered constant. The optimum choice of dead-time, t_{Dead}, is

$$I_L = \frac{2C_{Sw}V_{CC}}{t_{Dead}} \tag{5}$$

SIMULATION

The influence of ZVS on THD is investigated using Matlab/Simulink. A simulation profile using the Simscape toolbox is given in figure 2. The ode23t solver is used together with a minimum step size of 10 nS. Simulation data is resampled before performing FFT (Fast Fourier Transform) analysis. Open-loop operation is considered. A series resistance of 10 Ω is added to the output filter inductor in order to provide damping. The power stage parameters used for the simulation are identical to the ones of the experimental setup. This setup will be presented in the next section, and the key parameters are collected in table 1.

Figure 3 and 4 shows the spectrum of the output voltage at a modulation index of 0.9 and reference frequency of 1 kHz. In Figure 3, $t_{Dead} = 100$ nS and $C_{Sw} = 100$ pF, while figure 4 uses $t_{Dead} = 200$ nS and $C_{Sw} = 200$ pF. Significant uneven harmonics are observed in both figure 3 and 4. The simulated THD is 0.24 % and 0.48 %, respectively.

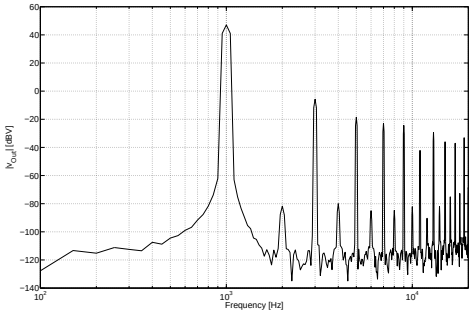


Figure 3: *Spectrum of output voltage ($C_{Sw} = 100$ pF and $t_{Dead} = 100$ nS).*

Figure 5 shows the simulated THD for three different sets of C_{Sw} and t_{Dead}. Clearly, the dead-time distortion can not be ignored under ZVS.

EXPERIMENTAL RESULTS:

Experimental measurements are performed on a 100 Var self-oscillating class D audio amplifier build around a half-bridge power stage. A hysteresis based bandpass current mode control (BPCM) scheme is utilised as an efficient way of implementing active damping of the second order output filter resonance, while ensuring high

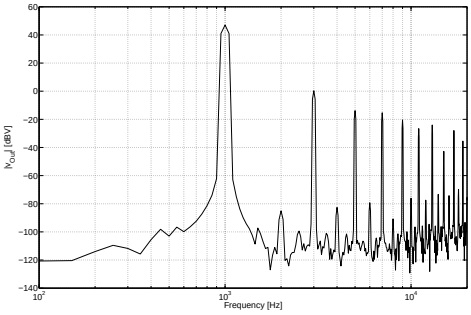


Figure 4: *Spectrum of output voltage ($C_{Sw} = 200$ pF and $t_{Dead} = 200$ nS).*

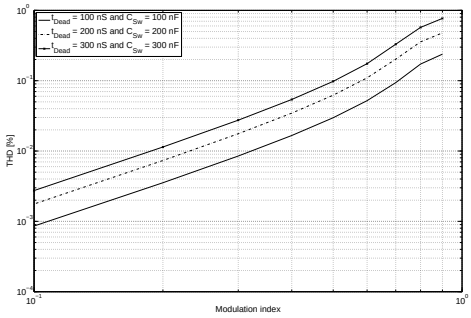


Figure 5: *Simulated THD.*

loop-gain. Key-parameters are collected in table 1. Two identical amplifier are constructed, one using Si MOSFETs STW4N150, while the other is using the SIC MOSFETs SCT2450KEC. Parameters of the two MOSFETs are gathered in table 2 and 3. Figure 6 shows the two test subjects. The STW4N150 MOSFETs were driving by a 18 V gate-source voltage, while the SCT2450KEC MOSFETs, were driving by a gate-driver having a supply voltage of -4.5 V to 22.5 V. Measurements are preformed at a supply voltage of plus/minus 500 V. The idle switching frequency is kept constant for both amplifiers at 100 kHz.

THD+N is measured using an APX525 audio analyzer and a voltage attenuation interface. The voltage attenuation interface is necessary in order to protect the input-stage of

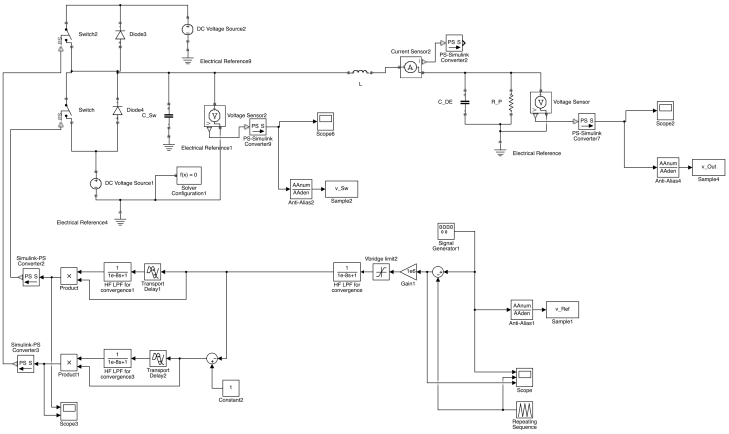


Figure 2: *Simulink profile.*

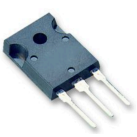
the audio analyzer. Measured THD+N is in figure 7 and 8 for the two test subjects of SCT2450KEC and STW4N150 as function of the reference voltage. Assuming voltage mode control the reactive output power will change with reference frequency, making it unsuitable to plot THD+N as function of power. Measurements are given for the reference frequencies of 100 Hz and 1 kHz. A midrange application is considered (100 Hz – 3 kHz).

From figure 7 and 8 two key observations can be made. The noise-floor is significant worse for the SiC MOSFETs, than that of the Si MOSFETs. In the region where THD dominates (high modulation index/reference voltage) the two types of MOSFETs performance identically. Both figure 7 and 8 shows THD+N of 0.3 % at a reference voltage of 1 V and frequency of 1 kHz. ZVS operation at idle is utilized for both MOSFETs. Note, that C_{Sw} is a function of not only the MOSFETs drain-source capacitance, but also the series connection of the output inductor interwinding capacitance and output capacitance, together with the heat-sink capacitance. Especially the output filter interwinding capacitance contributes signifanctly to C_{Sw}, causing C_{Sw} to be considered identical for both MOSFETs. Consequently the distortion, arising from the dead-time need to ZVS, must be identical.

Note that no absolute comparison can be made between the results of figure 7, 8 and 5. This is due to the fact, that open-loop operation is assumed in the simulations, while closed-loop operation is used for the measurements.

Table 1: *Power stage parameters*

	Designator	Value
Idle switching frequency	f_{Sw}	100 kHz
Output filter inductance	L	600 uH
DE Capacitance	C_{DE}	100 nF
Supply voltage	V_{CC}	$\pm$ 500 V
Closed-loop gain	A_V	48.9 dB



(a) STW4N150.

(b) SCT2450KEC.

Figure 6: *Test subjects.*

Table 2: *Parameters of STW4N150.*

	Designator	Value
On resistance	R_{DS}	7 Ω
Drain-source capacitance at 40 V	C_{DS}	100 pF
Gate-charge at v_{GS} = 12 V	Q_G	35 nC

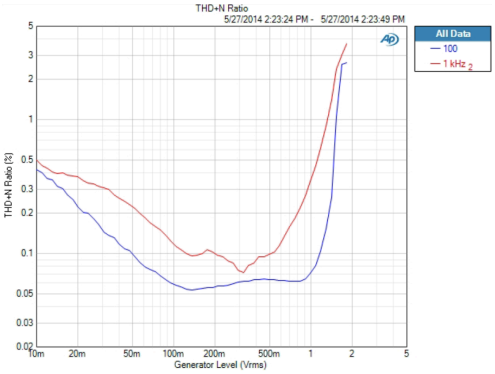


Figure 7: *THD+N (100 Hz and 1 kHz) for the STW4N150 MOSFETs.*

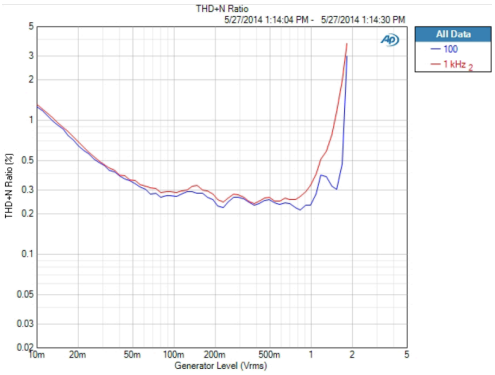


Figure 8: *THD+N (100 Hz and 1 kHz) for the SCT2450KEC MOSFETs.*

CONCLUSION:

The theory of pulse timing errors are revisited for the class D amplifier driving a capacitive transducer. Capacitive transducers are most known from their usage in electrostatic loudspeakers, however Dielectric Electro Active Polymers (DEAP) and piezoelectric ceramic can also be used to form a capacitive transducer. The high voltage requirements of capacitive transducers greatly reduces the option for suitable Si MOSFET. As a consequence it is investigated, if SiC MOSFETs could represent a valid alternative. It is shown, that at the present the technology of SiC MOSFETs can competitive with that of the Si MOSFETs in terms of THD, however the noise floor is significant higher for the SiC MOSFETs.

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Table 3: *Parameters of SCT2450KEC.*

	Designator	Value
On resistance	R_{DS}	450 m Ω
Drain-source capacitance at 1000 V	C_{DS}	20 pF
Gate-charge at v_{GS} = 12 V	Q_G	18 nC

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Thomas Haggen Birch, Dennis Nielsen and Arnold Knott, "Pre-distortion of audio circuits", 137 AES Convention, LA, USA.

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Pre-distortion of audio circuits

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ABSTRACT

Some non-linear amplifier topologies are capable of providing a larger than one voltage gain from a limited DC source, which could make them suitable for various, but especially mobile, applications. However, the non-linearities introduce a significant amount of harmonic distortion (THD) but some of this distortion could be reduced using pre-distortion. This paper suggests a linearising of non-linear audio amplifiers using a analogue pre-distortion approach. Initial results shows that a significant reduction in THD is obtainable using this approach and a prototype is constructed in order to verify this.

1. INTRODUCTION

Switch mode amplifiers have gained significant popularity during the last decades, mainly due to their high efficiency, decent audio quality and small bill of materials. The traditional approach have been to use the well proven buck topology. Benefits of the buck topology includes their ideally very linear DC-DC behaviour and it is a well tested and tried topology. However, the buck topology have a voltage gain limited to 1 with a half bridge or 2 for a full bridge. If an application, like automotive audio reproduction and other mobile sonic systems, requires a high voltage output but only offers a low voltage as a source, a high voltage gain could be useful. Instead of adding an additional step up converter, an amplifier design based on a different topology that the buck could be used.

Many different topologies provide higher voltage gains that the buck, such as the class-E[1] or SEPIC[2], just to name a few, but they come at the cost of being inherently non-linear. While non-linearities are a minor concern in certain applications, it is of great importance in high quality signal reproduction, due to the fact that high levels of harmonic distortion (THD) is introduced.

1.1. Pre-distortion

Many different approaches can be used to enhance linearity of an amplifier, with negative global feedback being a well proven and solid approach. The approach taken in the paper is based on a different concept. An additional non-linearity, tuned to be

the reciprocal of the amplifier non-linearity, is introduced intro the signal chain which linearise DC-DC transfer characteristics of the combined system. Fig. 1 show a combined system, where (A) is the pre-distortion, (B) is the amplifier characteristic and (C) is the collected response. Pre-distortion is a fitting

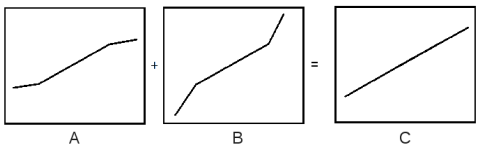

Fig. 1: The pre-distortion combined (A) with the amplifier (B) results in the collected response (C)

name since the introduced non-linearity is per definition introducing harmonic distortion and the technique is widely used in satellite communication and RF amplification[3][4]. Several different implementations exists of pre-distorters both in the discrete[5] and analogue[1] realm but an analogue approach have been chosen for this investigation, since it offers a potential significant sonic improvement with relatively few components.

1.1.1. Non-linear topologies for audio amplification

A large number of topologies are capable of delivering higher voltage gains than that of the buck. Work have gone into utilizing some of these topologies for audio reproduction, with[6] being a major contribution. It is suggested in[6] that two Cuk converters combined could be used in a audio amplifier design.

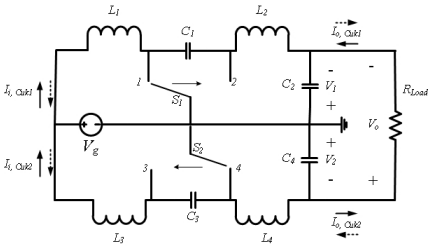

Fig. 1: The bi-directional Cuk converter

While providing a higher gain, reduced current ripples and a simple design/ low component count are amongst the stated benefits. Fig. 1 shows the schematic of a bi-directional Cuk suited for audio amplification and the DC-DC transfer characteristic of the bi-directional Cuk is given by Eq. 1

$$\frac{Vo}{Vi} = \frac{D-(D-1)}{D(1-D)} \tag{1}$$

Eq. 1 is plotted in Fig 2 and it can readily be seen that when the duty cycle,D, approaches its outer regions, e.g $D \to .01$ or $D \to 0.9$, the gain characteristics changes dramatically.

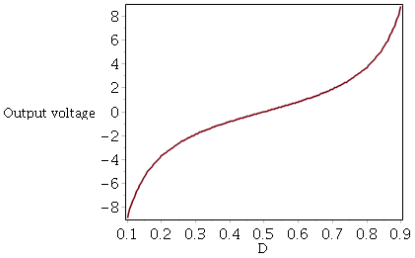

Fig. 2: The DC transfer fucntion of the bi-directional Cuk converter

2. PROPOSED CIRCUIT

The proposed compensation circuit is shown in Fig. 3

It consists of two diode coupled MOSFETS, M1, M2, two bias supplies, V_{bias},V_{bias2} and two resistors, R_{in} and R_{out}. Channel length modulation along with all conduction resistances and parasitic capacitances for the MOSFETs have been neglected in the following.

The circuit can be divided into different phases, depending on the value for V_{in}. V_{point1} is defined as the value of V_{in} where M1 turns on and V_{point2} as the value of V_{in} when M2 turns on.

2.1. Phase a

If $V_{point2} < V_{in} < V_{point1}$ then both MOSFETs are off. This reduces the circuit to a voltage division between R_{out} and R_{in} as shown in Fig. 4 and the output voltage is given by

$$V_{vout_a} = V_{in}\frac{R_{out}}{R_{out}+R_{in}} \tag{2}$$

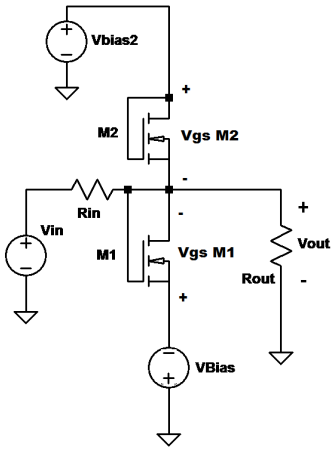

Fig. 3: Proposed non-linear circuit

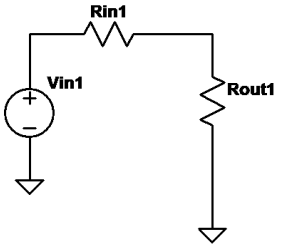

Fig. 4: Circuit in phase a

2.2. Phase b

When V_{in} rises so does V_{out}. This implies that the voltage difference between V_{bias} and V_{out} also rises since

$$V_{gs_{M1}} = V_{th_{M1}} = -V_{out} - V_{bias1} \tag{3}$$

M1 turns on when $V_{gs_{M1}}$ reaches the threshold voltage $V_{th_{M1}}$. Now current starts to flow in M1. The circuit can now be describes as shown in Fig. 5.

M1 is now described as a voltage dependant current source removing current from the output node. The current removed from the output node is equal to the drain current from the MOSFET. The Shichman Hodges model of an MOSFET in the active region gives an expression of the drain current i_d:

$$i_d = k(V_{gs} - V_{th})^2 \tag{4}$$

$$k = \frac{1}{2} C_{ox} \mu \frac{W}{L} \tag{5}$$

with square relationship between the drain current and V_{gs}. Eq. 3 determines that V_{gs} is related to V_{out}

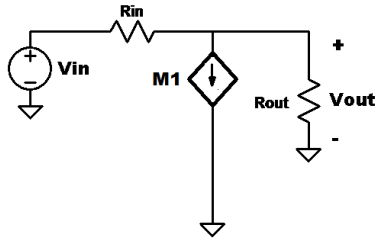

Fig. 5: Circuit in phase b

The output voltage can now be found by writing up a nodal equation of the currents in circuit shown in 5 which yields Eq. 8:

2.3. Phase c

When the input signal falls, the voltage difference between the gate and source of M2 increases. M2 turns on when $V_{gs_{M2}}$ reaches the threshold voltage $V_{th_{M2}}$.

$$V_{gs_{M2}} = V_{th_{M2}} = V_{bias2} - V_{out} \tag{7}$$

Now current starts to flow in M2. The circuit can now be describes as shown in Fig. 6. Now, the current in the active MOSFET M2, is flowing into the output node contrary to phase b. The nodal equation of the circuit shown in Fig. 6 is written up and solved for V_{out} which produces Eq. 6:

This yields an model which describes the circuit behaviour over a range of input voltages V_{in}

2.4. Summary of gain reduction circuit

Transistor characteristics in the $k = \frac{1}{2}(C_{ox}\mu\frac{W}{L})$ determines the amount of current through the transistors at a given V_{gs} and thus the amount of gain

$$\frac{V_{in}-V_{out}}{R_{in}} = -k(V_{gs}+V_{th})^2 + \frac{V_{out}}{R_{out}}$$
$$V_{out} = \frac{1}{2}\frac{1}{kR_{out}Rin}(2kR_{in}V_{th}R_{out} + 2kR_{in}R_{out}V_{bias} - R_{in} - R_{out} + (4kR_{in}^2V_{th}R_{out} + 4kR_{in}^2R_{out} \quad (6)$$
$$V_{bias}+4kR_{in}V_{th}R_{out}^2 - 4kR_{in}V_{in}R_{out}^2 + 4kR_{in}R_{out}^2V_{bias} + R_{in}^2 - 2R_{in}R_{out} + R_{out}^2))^{\frac{1}{2}}$$

$$\frac{V_{in}-V_{out}}{R_{in}} = k(V_{gs}+V_{th})^2 + \frac{V_{out}}{R_{out}}$$
$$V_{out} = \frac{1}{2}\frac{1}{kR_{out}Rin}(2kR_{in}V_{th}R_{out} + 2kR_{in}R_{out}V_{bias} - R_{in} - R_{out} + (-4kR_{in}^2V_{th}R_{out} - 4kR_{in}^2R_{out} \quad (8)$$
$$V_{bias}-4kR_{in}V_{th}R_{out}^2 + 4kR_{in}V_{in}R_{out}^2 - 4kR_{in}R_{out}^2V_{bias} + R_{in}^2 + 2R_{in}R_{out} + R_{out}^2))^{\frac{1}{2}}$$

reduction applied by the circuit when in phase b or phase c. To illustrate this, a conceptual DC-DC plot for different values of k is generated and shown in 7. It is clear from Fig. 7 that when the k parameter is increased the amount of gain reduction applied increases.

Either the bias voltages or the threshold voltage V_{th} can be used to determine the point where the circuit should leave phase a and enter either phase b or c. If the circuit is considered to be in phase a,where V_{out} is given by Eq. 2, Eq. 3 and 7 can be solved for either V_{th}or V_{bias} to find the transition point.

Input and output resistances also have an influence on the gain in phase b and c but R_{in} and R_{out} should have a large $\frac{R_{out}}{R_{in}}$ ratio since ideally no gain reduction should occur when the circuit is in phase a.

2.5. Reduced expression

However, when choosing the the components, a simpler expression is more convenient. If the output impedance is neglected and the MOSFETs are modelled by a voltage controlled current source depending on the transconductance, according to the small signal model of MOSFETs, the circuit can be reduced. This reduced circuit is shown in Fig. 8

Writing up the nodal equation and solving for V_{out} and differentiating with respect to V_{in} yields:

$$V_{out} = \frac{R_{in}V_{bias}gm + V_{in}}{Rgm+1} \quad (9)$$
$$\frac{\partial V_{out}}{\partial V_{in}} = \frac{1}{gmR_{in}+1} \quad (10)$$

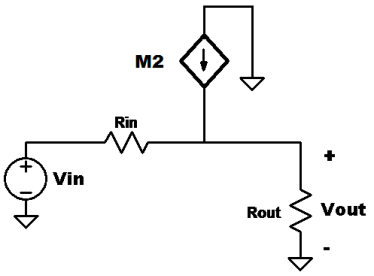

Fig. 6: Circuit in phase c

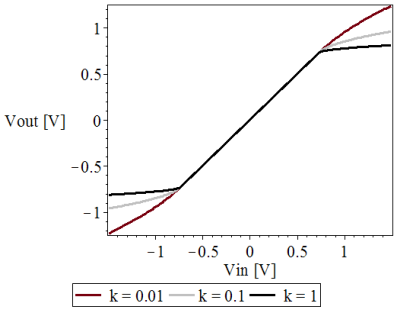

Fig. 7: The circuit show an increased gain reduction when k is increased

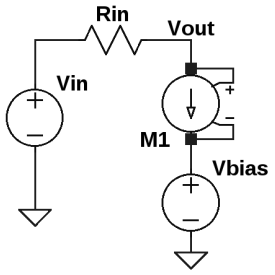

Fig. 8: Reduced circuit schematic

Eq. 11 thus estimates the slope and thus the gain of the pre-distorter based on a MOSFET with a certain gm parameter and for a given input impedance. It can also be seen that the input impedance, R_{in} can be effectively used to control the gain.

3. SYNTHESIS AND SIMULATIONS

The simulated circuit is normalized to a input voltage of $V_{in} \pm 1$ and the resulting DC response is shown in Fig. 9

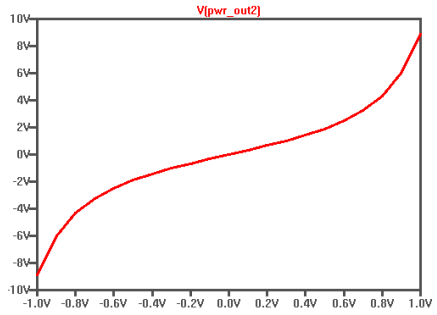

Fig. 9: The normalized DC response of the power stage

The slope just around $V_{in} = 0$ of DC response shown in Fig. 9 is found to be $3.2\frac{V}{V}$. This is the desired gain and the power stage must then maintain this slope for all input voltages. According to Eq. 1, the Cuk delivers a gain of 5.4 at $D = 0.85$. The desired linearised DC response requires a gain of 2.7 at this point which is achieved when $D = 0.75$. This means, in other words, that the pre-distorter should reduce the original input leading to $D = 0.85$ to and input producing only$D0.75$.

For the normalized power stage, an input of $V_{in} = 627mV$ yields a output of $2.7V$ and a $V_{in} = 870mV$ yields an output of 5.4. This implies that the pre-distorter should reduce an input voltage of $V_{in} = 870$ to $V_{out_{dist}} = 627mV$ to compensate for the power stage.

To find the necessary gm, a conduction point, meaning the point where the pre-distorter kicks in, is chosen and in this case it is chosen to $V_{in} = 0.5V$ since it is on the edge of linear region of the power stage. This allows for an regression between the two points of (0.5, 0.5) and (0.87,0.627), which yields a slope of $A = 0.34$ which is shown in Fig 10.

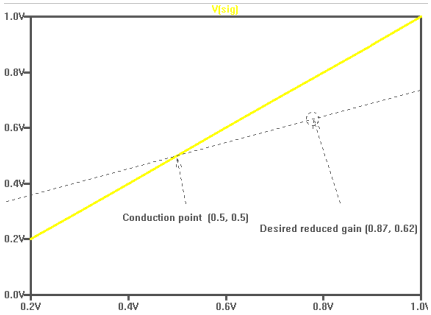

Fig. 10: The regression between two points, the yellow line represents the ideal input

Now, Eq. 11 can be used to find the necessary transconductance of the, but since the slope A is found for the normalized response, it has to be divided with two. A input resistor of 300Ω is chosen and the values are inserted into Eq. 11 which yields a gm parameter of $gm \approx 0.017$.

$$\frac{A}{2} = \frac{1}{gmR_{in} + 1} \tag{11}$$

$$gm = -\frac{A-2}{AR} \tag{12}$$

$$gm = 0.017S \tag{13}$$

Bias voltages are chosen to be $V_{bias} = \pm 0.8V$ which, according to Eq. 3 requires the threshold voltages of the MOSFETs to be 1.3V. The compensator response is plotted in Fig 11 and is added in the signal chain and the DC response is yet again simulated.

The result is plotted with the ideal response and shown in 12

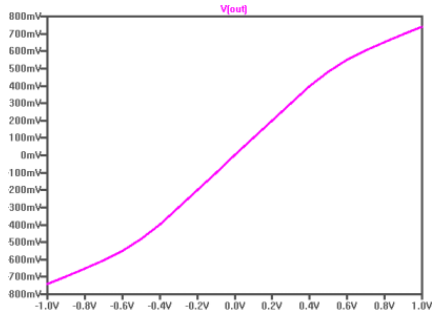

Fig. 11: The DC response of the compensator, normalized to an input range of $\pm 1V$

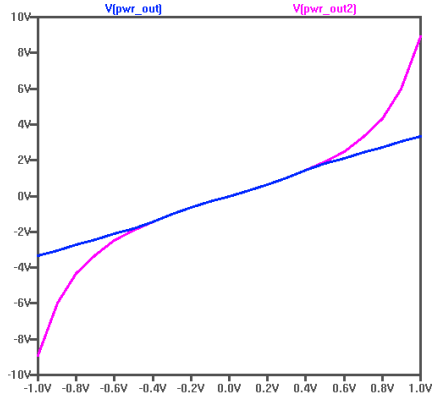

Fig. 12: The non-compensated (Purple) and the compensated(Blue) DC response of the power stage

The circuit is now simulated with a input sine with an amplitude 1V and results are shown in Fig. 13

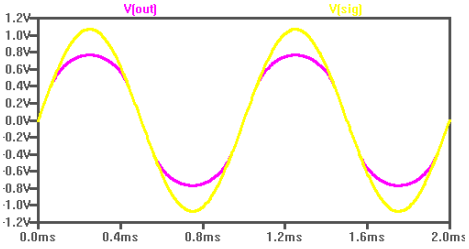

Fig. 13: The input voltage (Yellow) and the output voltage (Purple) of the compensator

Fig. 14 show the output voltages of a compensated power stage and a non-compensated power stage.

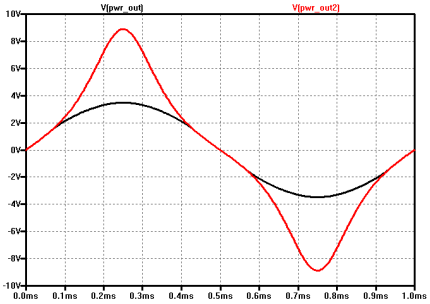

Fig. 14: The non-compensated (Red) and the compensated(Black) output voltages of the power stages.

An FFT spectrum analysis is performed on the output of the compensator with a 1V 1kHz sine wave. It is shown in Fig. 15. It can be seen that according to the simulation model, the odd harmonics are dominating while the even harmonics are well below 140dB. It is noted that the 13. harmonic is significantly lower that the rest of the visible harmonics.

A spectrum analysis for the output of the power stage is also conducted based on a simulation with a 1V 10kHz sine wave. The result is shown in Fig. 16

It can be seen that the frequency content is changed significantly, reducing the harmonics at 30Khz from -3dB down to -39dB. Based on the nine first harmon-

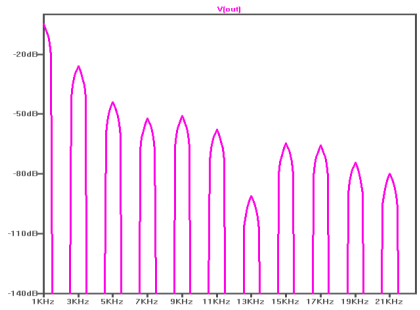

Fig. 15: The simulated result of the output voltage of the compensator

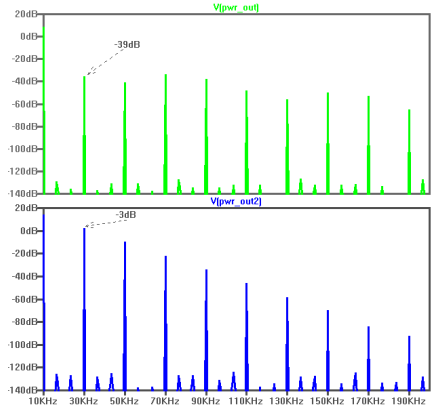

Fig. 16: FFT spectrum of the compensated (Green) and non compensated (Blue) output voltage from the power stage

ics, the THD for the uncompensated power stage is 25% and for the compensated 0.9%.

4. PROTOTYPE

A simple prototype of the circuit is build and shown in Fig. 17.

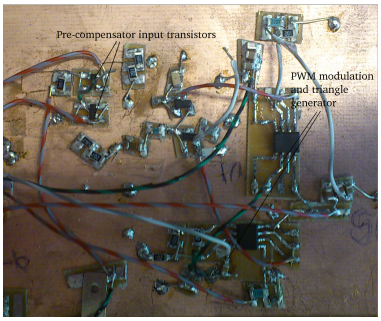

Fig. 17: simple prototype with PWM modulation for driving a power stage

A pair of BSS83 N-channel MOSFETs are used to construct the pre-distorter. They have a rated transconductance gm of $> 0.015ms$ at 1kHz for $V_{DS} = 10V$ and $I_D = 20mA$. Their threshold voltages are specified to lie within 0.1-2.0V and typically 1.3V. To achieve the correct conduction point, the bias voltages can be adjusted. The prototype is fed with a input sinusoidal with an amplitude of 1V. The result is seen in Fig. 18

It can be seen that the measure response and gain reduction show good correlation with the expected result from the simulations, with a reduction of $\approx 200mV$. When the pre-distorter is active, a significant amount of additional harmonics are expected. To investigate which harmonics are introduced, a FFT spectrum analysis is performed of the compensated input signal.

The spectrum differs from the expected simulated response showing significantly larger even harmonics compared with Fig. 15. This may have different origins such stray inductances or capacitances, but it remains to be investigated further.

5. CONCLUSION AND FUTURE WORK

A pre-distortion circuit adapted for the bi-

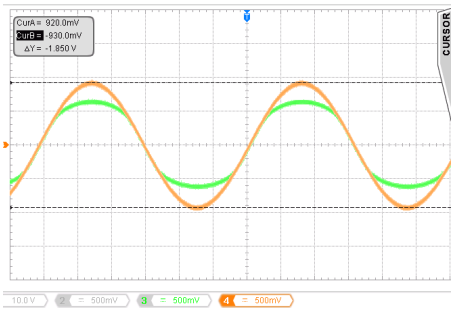

Fig. 18: The prototype, Yellow is the input voltage and the green is the compensated output voltage

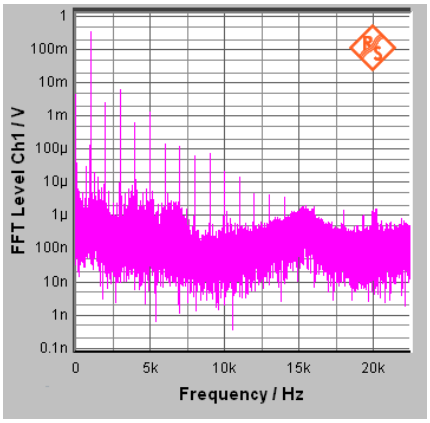

Fig. 19: Odd harmonics are emphasized when the compensator is active

directional Cuk converter have been suggested. It has been described mathematically, both using the Shichman Hodges model and the small signal model. Simulations suggests that a a reduction from 25% to $\approx 1\%$ is possible. A prototype have been build and it shows good correlation with simulations and initial calculations but with some differences in the frequency spectrum. All IC components are subject to process variations, which changes the actual parameters of the components. Designing a current controlled version of the compensator could overcome these variations, and could allow for a much more precise control of the circuit.

The next step is to finish the prototype power stage and test the pre-distortion circuit with this to verify if or not an improvement of THD is observable.

The concept of pre-distortion is well proven and described in literature, and provides an easy and cheap improvement of linearity. Many other non-linearities are found in audio amplifier systems and this concept could also be used to compensate for other types of non-linearities, such as dead-time or carrier distortion.

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